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CHIPSEAL â INORGANIC SEALING TECHNOLOGY FOR HERMETIC-LIKE INTEGRATED CIRCUITS

VOLUME 1

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1. Executive Summary

Technology advancements in semiconductor device design and fabrication have led to significant improvements in information processing capacity and speed. However, when devices are required to operate under severe environmental conditions, a significant portion of the capability is lost because of the need to place the device in an external hermetic enclosure. The characteristics of this type of package limit the packaging density and electrical performance of the enclosed microcircuit. The explosive growth in consumer electronics has significantly shifted the packaging of integrated circuits (ICs) away from hermetic enclosures to the use of lower cost plastic packaging configurations. Unfortunately, traditional plastic packages have not provided the long-term reliability needed for military applications. A new thin-film wafer processing technology known as ChipSeal Inorganic Coatings has been developed which can provide hermetic-equivalent performance for bare IC die and plastic encapsulated ICs and is compatible with all electronic interconnect methodologies used for single-chip or multichip applications.

ChipSeal is an advanced inorganic passivation system that is deposited at the wafer level from "molecular designed" silicon materials using standard semiconductor processing technology. A spin-on, flowable, oxide film is first deposited from a novel silica precursor, hydrogen silsesquioxane, which planarizes the surface. A plasma-silicon carbide (SiC) film is then deposited from a single source, nonpyrophoric, trimethylsilane gas. The plasma-SiC is resistant to chemical attack and moisture adsorption, provides high scratch resistance, and has excellent thermal expansion match to the silicon substrate. These dielectric materials are combined with a high reliability (high-rel) noble bondpad metallization to produce a more robust IC for advanced packaging applications. The thin-film structure of ChipSeal compared to a standard IC device is shown in Figure 1.

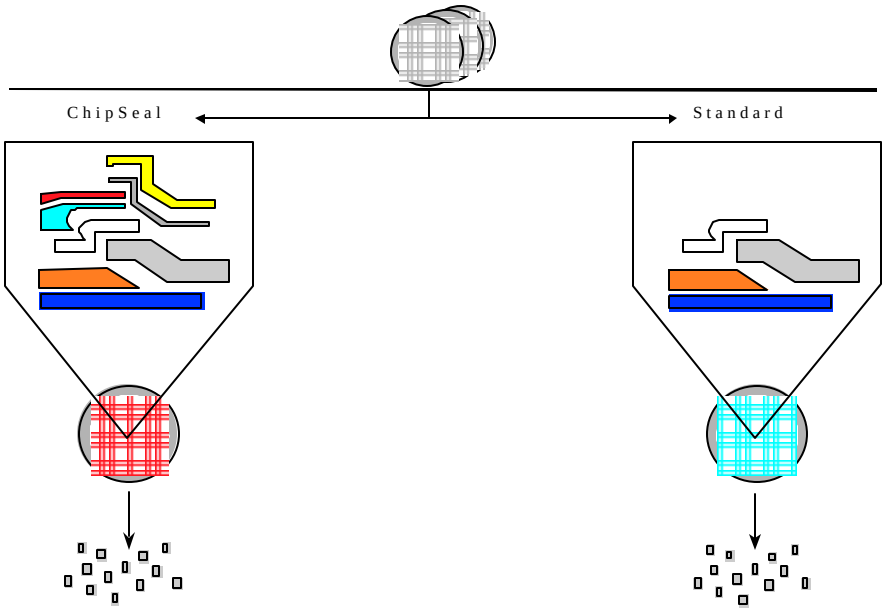


Figure 1. ChipSeal Processing versus Standard Processing

The program was conducted in two phases by a diverse team of technology companies, specializing in different levels of the electronic packaging / equipment supply chain. Table 1 identifies the primary team of companies with their key contributions.

Table 1. ChipSeal Team and Each Company's Contributions

Company	Contributions
Dow Corning Corporation	Materials supplier; Program mgmt.
Chip Supply Inc.	Wafer/device testing; KGD
MCNC	Flip-chip solder bump integration development
Rockwell-Collins	MCM integrator
Sarnoff Corporation	Process development / wafer processing

In addition, many other companies also contributed to the results contained within this report since it was important to have third party validation of the test results and to leverage existing industry capability and infrastructure.

Phase I focused on the "proof-of-concept", which consisted of developing the base processes for application and etching of both the protective dielectric films and the high reliability contact metallization system. In addition, packaging, reliability testing and direct integration into solder bump processing were pursued. Phase II focused on the implementation of the technology through scale-up, wafer processing of a wide variety of commercial and proprietary device types, and plastic packaging reliability assessment. As an adjunct to Phase II, two demonstration multichip modules (MCMs) were designed, integrated, assembled and tested using a multifactorial experimental design with ChipSeal processed devices.

In Phase I, to demonstrate "proof-of-concept" of the hermetic-equivalence of the ChipSeal technology, the process was applied to a set of silicon IC devices. These were 1.5 µm, bipolar complementary metal oxide semiconductors (BiCMOS), double-level metal, gate array devices. After processing, wafer testing showed that the ChipSeal process equaled or improved the device yield when compared to control wafers. Control and ChipSeal processed wafers were then plastic packaged in standard surface mount, small-outline format. Additional control samples were hermetically packaged. Packaged devices were then subjected to and passed MIL-STD-883 screening and qualification tests. Packaged devices designated for environmental stress testing were subjected to sequential preconditioning per the Joint Electron Device Engineering Council (JEDEC) Method A113, followed by 140 ºC temperature/humidity/pressure and bias testing (also referred to as the highly accelerated stress test or HAST) to assess device reliability. Figure 2 shows the cumulative failures for 1000 hours of stress testing. The data clearly demonstrates the hermetic-equivalent performance of the plastic overmolded ICs with the ChipSeal processing.

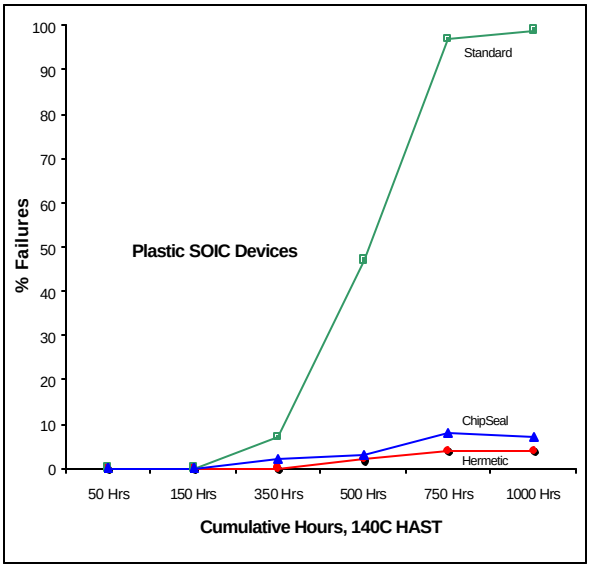


Figure 2. Comparative HAST Results of Plastic Encapsulated Devices

To demonstrate the effectiveness of the ChipSeal technology for providing hermetically equivalent performance of bare die, a set of the same control and ChipSeal processed ICs were packaged in unlidded, ceramic leaded chip carriers. These devices were subjected to the same screening, qualification, preconditioning, and environmental stress testing as the plastic encapsulated devices. The results shown in Figure 3 again clearly indicate a hermetic-equivalent performance for unencapsulated ChipSeal processed devices. This result provides further verification that the ChipSeal process can provide the level of environmental protection required for optimum flexibility and utilization of bare die in a wide variety of packaging formats.

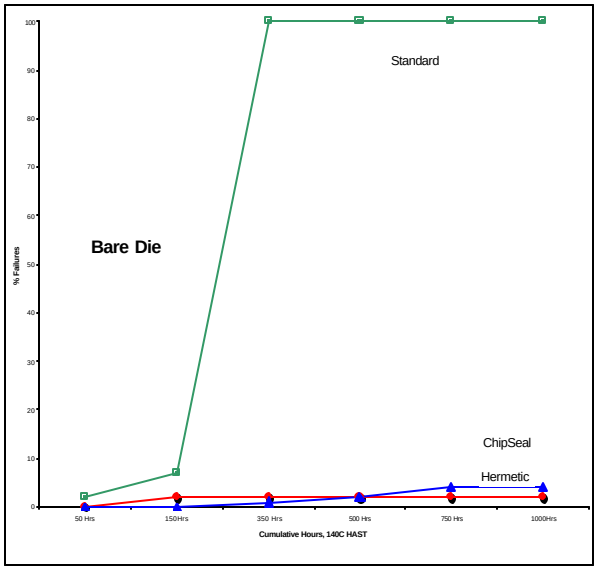


Figure 3. Comparative HAST Results of Bare IC Die

One of the advanced packaging technologies which could benefit the most from the use of hermetic-equivalent thin film protection are application specific electronic modules, also known as MCMs. In their preferred configuration, MCMs will be assembled using flip-chip solder bump interconnect technology. To demonstrate the compatibility of ChipSeal with solder bump processing, sample devices were processed using standard under bump metallization (UBM), solder plating and reflow techniques. To provide a reliable interface for testing, the plasma-SiC was also applied to interconnect designs prepared on silicon substrates. However, only qualitative reliability information could be obtained because of complications arising from mechanical limitations and damage of the silicon substrates upon insertion and removal from the test sockets. Greater than 75 percent of the assemblies were functional or demonstrated continuity at initial electrical tests. Mechanical integrity and continuity of the bumps was maintained through burn-in tests. Temperature cycling and salt fog exposures did result in a significant decrease in mechanical strength and bump integrity. Although the results are inconclusive as to the factors contributing to the reduced reliability, the initial tests do indicate that the ChipSeal process is compatible with the flip-chip solder bump processing.

In Phase II, to demonstrate the compatibility of the ChipSeal process for a variety of device types, approximately 100 wafers of six different commercial and four proprietary devices were processed and tested to determine the effects of the process on device yield.. The commercial devices were chosen on the basis of function, gate geometry, and their applicability in the MCM technology demonstrator modules. The proprietary devices were submitted independently by various agencies or companies for evaluation of the ChipSeal process for their particular applications. The device types ranged from simple linear amplifiers to high speed digital microprocessors.

The ChipSeal passivation was deposited and etched on a specific quantity of wafers for each device type. Depending on the type of metallization required, the wafers were shipped via Chip Supply, Inc. to either the Microelectronics Center of North Carolina (MCNC) for solder bumping or a third party bump facility for gold bumping using the company's standard "proprietary" process but using the ChipSeal design rules. Standard 125 µm solder bumps were deposited, along with specific UBM, directly on the aluminum bondpads or a single mask redistribution process was used on fine pitch input/output (I/O) devices which employ 100 µm bumps. Standard 25 µm gold bumps were deposited, along with a titanium tungsten (TiW) barrier layer, directly onto the bondpads.

To assess the compatibility of the diverse types of semiconductor devices to the inorganic thin film coatings and processes, both the specific device manufacturer or ChipSupply, Inc was used to perform wafer level testing. Wafer level testing, also referred to as wafer probe, was completed before and after processing. Control wafers, which did not receive any subsequent processing, were also tested along with those processed to assess test repeatability. All of the results are reported using differential calculations to protect the manufacturers proprietary probe yield. All of the processed wafers showed some overall change in yield but varied widely by device type and metallization. The net change in yield of the control wafers was small, <5 percent, and is considered to be within the variability of the wafer probe itself. Wafers processed with the ChipSeal coatings showed a net change in yield of ~ 7 percent illustrating compatibility with a multiplicity of device types.

One of the devices from Phase II was selected for plastic encapsulation and reliability testing in cooperation with the device manufacturer, Rockwell Semiconductor. The device chosen was a 0.6 µm complementary metal oxide semiconductor (CMOS) microprocessor having 100 I/Os. A control (uncoated) and ChipSeal wafer were designated for assembly and molding in the manufacturers' plant using production materials and procedures. The package configuration was a 100 lead plastic quad flat pack (PQFP). The initial packaging yield for each group differed by less than 1 percent. A statistical sample from each group was submitted for moisture sensitivity evaluations and both qualified at JEDEC Method A112, Level 3, thus indicating no difference in the effect of the ChipSeal coating on the adhesion between the encapsulation compound and the die surface. The remaining parts were then submitted to Level 3 preconditioning. The parts were subdivided into three statistical groups for unbiased autoclave (121 ºC / 168 hours), temperature cycle (-65 to +150 ºC, 2000 cycles) and HAST testing (130 ºC, 85 percent relative humidity (RH), 1500 hours). There were no electrical failures for either group as the result of the autoclave and temperature exposures. As a result of the HAST exposure, for a total of 35 failures, the failure rate for the control and the ChipSeal groups was nearly identical (16/100 versus 19/100). Because of the low number of total failures and the small difference between groups, the results are considered inconclusive. ChipSeal processing did not degrade the intrinsic performance nor did it enhance the reliability for this particular "highly reliable" device. The overriding factor may be the very high integrity and moisture resistance of this particular manufacturers' package design and process controls.

Rockwell Collins conducted an MCM evaluation jointly with Dow Corning to evaluate any MCM assembly related benefits as well as the effectiveness of the ChipSeal coating on the environmental reliability of functioning circuits built on laminate substrates. All MCMs used a combination of surface mount technology (SMT) devices and bare die, with and without epoxy encapsulants. This effort was conducted with corporate internal research and development (IR&D) funds and is reported here for completeness. A Data Accumulator module was constructed using a combination of ten analog amplifiers and operational amp devices and a Global Positioning System (GPS) module was constructed using six devices, including a digital microprocessor, application specific integrated circuit (ASIC), fast static random access memory (RAM) and flash memory devices. The bare die used for these modules were selected from the ChipSeal processed and un-processed control wafers from the process compatibility study. All devices were subjected to known good die (KGD) screening before module assembly to optimize assembly yields. Both encapsulated and unencapsulated ChipSeal and control modules were subjected to various environmental reliability tests. For the vibration tests (incremental exposures up to 53 G_{rms}), temperature cycling (1000 cycles, –55 to +125 °C), and high humidity tests (up to1000 hours, 85 °C/85 percent RH/5V), there were no failures attributable to ChipSeal processing. The failures that did occur in the temperature cycling or vibration tests occurred as a result of mechanical failures of the solder joints between the module substrate and the printed test board. For the high humidity tests, the ChipSeal protected ICs survived 1000 hours of exposure without failure while the control modules experienced 10 to 30 percent failure rates during the same exposure.

The HAST exposures (up to 800 hours, 130 °C/85 percent RH/5V bias) revealed more discriminating results. Epoxy encapsulated die on the Data Accumulator modules, for both the ChipSeal and control modules, all failed within the first 200 hours of exposure; unencapsulated die modules revealed significant failures not occurring until 400 hours of exposure. The

ChipSeal modules showed single or multiple open circuit electrical failures that were attributed to corrosion of the underlying aluminum bondpad and separation (lifting) of the gold bump from the barrier metallization (TiW). For the control modules, the failures were attributed to severe corrosion of the aluminum bondpads that, in some cases, extended under the passivation and along the die traces. Corrosion was also observed in central regions of die, attributed to flaws in the primary passivation, that were not observed for the ChipSeal coated die. A similar situation was observed for the GPS modules.

The module data suggests that a contributing factor to the HAST failures appear to be the use of epoxy encapsulants (acid anhydride curatives) or plastic laminate substrates. This has not been well documented in the literature, since HAST is a relatively new reliability test method, especially for MCMs, but is clearly an area requiring followup. An underlying concern is that the high reliability metallization did not provide the level of protection expected when used in a direct chip attach architecture. Multiple hypotheses could account for the failures that were caused by the ingress of moisture and corrosive ions including the following:

- Residual contaminants from wafer processing/etching.
- Contamination of the aluminum bondpad prior to deposition of the metallization system due to handling, packaging and shipping between processing facilities.
- Degradation of the interface between the plasma-SiC and the metallization system caused from the undercutting of the TiW during wet etch processing, resulting in a buildup of localized high stresses along the interface.
- Prior experimental data showed the importance of process control with respect to the amount of nitrogen moiety within the TiW barrier layer. Nitrogen can backfill into the sputtering chamber and become incorporated into the TiW film (i.e. TiWN), leading to a reduction in adhesion properties to both the gold layer as well as the substrate.
- Film stress of the deposited TiW metallization has been shown to differ significantly between runs from the same sputtering tool as well as from different tools. High film stress leads to delamination (adhesion loss) of the films at the interface.
- Probe marks were evident on all wafers prior to processing which reduces the coverage and effectiveness of the TiW barrier layer. Gold in direct contact with aluminum produces intermetallic formation (Kerkendall voiding) and is more susceptible to corrosive attack under adverse conditions.
- Degradation of the metallization stack from KGD soft tape automated bonding (TAB) bond/de-bond processing.

In the hypotheses cited, moisture and ionic ingress at the metal-dielectric interface or within the metallization stack can contribute to the degradation of the electrical contact. There is insufficient data to substantiate the MCM failures at this time; additional effort is required. Lack of corrosion failures within the central areas of the ChipSeal processed die indicates that the ChipSeal dielectrics can provide the protection desired.

The following tasks have been identified for further development:

1. Determine the exact mechanism of the corrosion failures observed in the MCM evaluations.
2. Investigate barrier layer integration:
   a. Run to run variability

   b. Tool to tool variability
   c. Key contaminants
   d. Interfacial and microstructural properties
   e. Vertical sidewall etch processing to prevent undercutting
3. Identify and evaluate alternate metallization systems for use with potentially corrosive encapsulation systems.
4. Investigate integration with flip-chip solder bump:
   a. The nature of many failures was different but the number of failures was similar.
   b. Complete evaluations of flip-chip metallization structures in HAST with and without encapsulants is recommended.

In summary, the ChipSeal process demonstrated near hermetic performance when applied to the 1.5 µm BiCMOS devices in both bare die and plastic encapsulated package configurations. The ChipSeal process also demonstrated compatibility with a wide variety of commercial devices as evidenced by negligible effects on device wafer yields. The process is shown to be compatible with commercial plastic packaging materials and practices, flip-chip interconnect materials and processes, and KGD screening procedures. The ChipSeal process demonstrated compatibility with MCM assembly approaches, but the metallization system did not provide the degree of environmental protection desired when exposed to HAST conditions in the presence of cure-in-place epoxy encapsulants. The cause of the module electrical failures was identified as corrosion of the aluminum bondpad and/or separation of the diffusion barrier metallization (TiW) from the gold bump. It is thought that corrosive contaminants, leached from the epoxy, contributed to the module failures that were not present in the previous reliability evaluations. Further improvement of the metallization system is needed for module applications requiring hermetic-equivalent performance.

Although this program, the program team and its sponsors, produced many technological accomplishments, in retrospect, we probably moved too quickly. Phase II was expanded in scope with insufficient resources to effectively investigate all of the variables necessary to be completely successful. This undoubtedly leaves questions and issues unresolved that would require additional developmental effort. But one thing is clear: the technology developed and implemented in this program illustrated the ability to integrate the ChipSeal technology into both existing and next generation electronic packaging applications for military microelectronic systems.

1.1 *Program Accomplishments*

1.1.1 Phase I

- Demonstrated successful integration of the ChipSeal protective coating process with standard industry IC manufacturing technology.
- Demonstrated hermetic performance of ChipSeal processed ICs for both plastic encapsulated and bare die packaging configurations.
- Demonstrated compatibility with both wire bond and solder bump interconnect approaches.
- Materials and processes successfully transferred to other process facilities.
- Processes successfully developed for 100 mm wafer size.

1.1.2 Phase II

- Processes successfully scaled to 150 mm wafer size.
- Process compatibility demonstrated for 10 device types, including analog, digital and memory ICs.
- Compatibility with current production PQFP packaging methodology demonstrated.
- Package reliability assessment demonstrated no negative effects of the ChipSeal processing.

1.1.3 MCM Evaluations

- Demonstrated compatibility of ChipSeal processed ICs with KGD screening procedures typically used for MCM assembly operations.
- Demonstrated the robustness of ChipSeal processed ICs with temperature cycling and vibration tests used for the evaluation of MCMs.
- Demonstrated improved reliability for ChipSeal processed die in biased high humidity tests.
- Demonstrated elimination of pinhole corrosions failures for ChipSeal processed die that can occur in standard IC passivations.
- Identified weaknesses in the high reliability metallization system when used with chemically cured encapsulants exposed to HAST conditions.

1.1.4 ChipSeal Process Benefits

- Lower cost compared to other external hermetic packaging approaches.
- Packaging is performed in a cleanroom environment using standard semiconductor processing tools and procedures.
- Reliability is built into the device using thin film packaging.
- Compatible with a wide variety of IC device types.
- Compatible with other semiconductor types including gallium arsenide (GaAs) and silicon-on-sapphire (SOS).
- Applicable to high reliability commercial or defense products.
- Compatible with high efficiency interconnect methodologies, including flip-chip and tab bonding.
- Compatible with KGD test methods.

An executive overview of the ChipSeal Inorganic Sealing Technology for Hermetic-like Integrated Circuits is shown in Figure 4.

DOW CORNING

Executive Overview

ChipSeal® Inorganic Sealing Technology for Hermetic-Like ICs

Objective

The objective of the program is to develop hermetic-like thin film coatings on integrated circuits at the wafer stage and demonstrate the compatibility and performance on commercial IC devices.

Program

Two Phases focused on:

I. Process Development and Deployment
- Proof-of-concept
- Reliability Assessment
- Solder Bump FC Integration

II. Demonstration on Commercial Devices
- Scale-up to 150 mm
- Device Compatibility / Wafer Processing
- PEM & MCM Packaging and Assessment

Benefits

- Applicable to a range of semiconductor and device types including Si (both analog and digital), GaAs, and SOS.
- Hermetic sealing is performed at the wafer level in a cleanroom environment using standard semiconductor processes and equipment.
- Robust IC protection for ruggedized applications.
- Dual Use
- Lower cost compared to external packaging solutions.
- Invariant to package design (integrates readily into PEMs and MCMs).

Technology

- Advanced Inorganic Dielectric Passivation
  - Spin-on, Low K, Planarizing SiOx Dielectric
  - PECVD Barrier, Low K a-SiC:H Dielectric
- High Reliability Metallization System
  - KGD Compatible – Gold Bumps
  - Flip Chip Solder Bumps – Thin Film Gold
- Wafer Level Processing Which Leverages Existing IC Fabrication Equipment and Infrastructure.

Figure 4. Executive Overview of ChipSeal Inorganic Sealing Technology for Hermetic-Like Integrated Circuits

2. Introduction

Trends in the commercial electronics market have pushed semiconductor manufacturers to develop smaller and faster circuits at lower cost. The manufacturers have met the challenge by shrinking transistor dimensions, integrating more functions on a single chip, and reducing package size and cost. These improvements have resulted in explosive growth of ICs in consumer electronics. An essential element of this growth has been the use of plastic packaged ICs. To further the trend toward even smaller, faster, and cheaper electronics, manufacturers are now adopting wider use of chip-scale packages and MCM technology for chip-on-board (COB) type of assemblies. Although the general trend is of benefit to all systems, packaging approaches intended for commercial applications do not provide the environmental reliability suitable to military, aerospace, and industrial applications.

For decades, the means to achieve the required reliability has been the choice or specification of hermetic packages. Hermetic packages are constructed of a pressed or laminated ceramic with internal metallized or glass bonded leads and external side-brazed pin attachments. The package is sealed with a metal or ceramic lid that is bonded with a low melting glass. However, the use of hermetic packages presents limitations in terms of size, weight, performance, and cost that are as undesirable for military systems as they are for commercial use. Also, as semiconductor manufacturers are increasingly driven to deliver more products for the commercial markets, the manufacturing capability and availability of hermetically packaged ICs has rapidly declined. A solution to this dilemma is to develop chip protection technologies that will provide hermetic-equivalent performance while being compatible with commercial applications.

Significant improvements have been made in conventional plastic packaging molding and encapsulation materials and processes. Improvements in expansion characteristics, modulus, adhesion, and purity, have led to improved robustness. In some cases plastic packages from well-controlled processes are “good enough” to be used in applications formally reserved for hermetic assemblies. However, most plastic encapsulated microcircuits (PEMs) have been developed for high volume, low cost consumer electronic applications in which long term environmental reliability is not a concern. Recent directives to use more commercial-off-the-shelf (COTS) packaged devices for critical military applications have raised the concern over how good is “good enough”. Commercial devices are usually only required to survive near-room-temperature humidity conditions or relatively low temperature unbiased autoclave tests. Hermetic devices, in contrast, must withstand biased high temperature/high humidity tests for up to 1000 hours. An approach to achieving hermetic performance in an unknown plastic encapsulation is to provide the hermetic-equivalency at the chip level.

Even if individually plastic packaged ICs can provide hermetic performance, they also incur the penalties for size, weight, interconnect lengths, slower processing speeds, reduced temperature capability, and/or higher power consumption. Hence, the trend in IC design and manufacture is to incorporate more functional elements onto one chip. Although this approach can be effective for large volume commercial applications, it reduces design versatility, increases lead times and can significantly increase costs for small volume military system needs. The solution is to combine multiple bare chips on a single substrate, MCMs, using conventional wire bonding or high density interconnect approaches such as flip-chip. For this approach to succeed the individual chips must be KGD and must also be able to withstand the environments imposed on their hermetic counterparts, i.e., they must stay good for the life of the system. Although the

module itself could be sealed in a hermetic package, the same penalties of size, weight, and cost are incurred.

Dow Corning has developed a new thin film passivation technology known as ChipSeal Hermetic Coatings that completely seals an IC chip against moisture and corrosion using advanced materials less than 1 μm thick. When used with a high reliability metallization, the combination provides a hermetic-equivalent IC that is compatible with all interconnect methodologies for single chip and multichip packaging applications. This report presents the results of a three-year effort sponsored in part by the Air Force Research Laboratory to demonstrate and implement the technology for military ICs. The activities included the application and environmental evaluation of the ChipSeal coatings on test devices, the demonstration of the compatibility of the process on a variety of commercial and proprietary IC devices, and a comparative evaluation of the performance in MCMs and PEMs. The scope of the program involved a wide range of activities encompassing process development, concept demonstration, scale-up from 100 to 150 mm wafer formats, implementation and compatibility evaluation on a variety of device types, KGD evaluation, and packaging integration and assessment.

3. Background

It is well recognized in industrial, automotive, and government applications that moisture and ionic surface contaminants are the major contributors to the failure of ICs through electrochemical and direct corrosion mechanisms. Where potentially damaging environments are known to exist, the solution has been to place critical microcircuits in hermetic packages to maximize the long-term reliability of the system. The penalties associated with this approach are reduced circuit performance and increased costs at the component, assembly and system levels.

The feasibility of using an inorganic coating technology applied directly to the microcircuit was first studied under the Defense Advanced Research Program Agency (DARPA) sponsorship (Contract No. F49620-86-C-0110) [1]. The original concept, Surface Protected Electronic Circuits (SPEC), involved the application of three inorganic protective layers using specific organosilicon precursors to derive SiO_x, plasma-SiC, and SiN_x on wire bonded ICs. Statistical quantities of GaAs and silicon CMOS circuits were used as test vehicles. The films were applied in thicknesses of 0.1 to 0.3 µm to assembled circuits in open, side-brazed, leaded chip carriers and evaluated against uncoated circuits in temperature cycling, autoclave, HAST and salt fog tests. The study showed that the SPEC coatings had no adverse effect on the circuit functions and clearly demonstrated improved circuit protection. Subsequent evaluations showed that the SiN layer did not contribute to the overall protection and was removed from the multilayer structure. The SiO_x and plasma-SiC coatings were applied at lower temperatures (250 °C) at slightly increased thickness (0.5 -0.6 µm) with a silicone gel top coating for mechanical protection. Reliability tests again demonstrated improved protection in autoclave, HAST, temperature cycle and salt fog testing in comparison to uncoated devices and devices coated with silicone gel alone. For the two-layer coating, only one coated device failed in HAST and, for the three-layer system, no coated devices failed after 500 hours exposure, whereas all but one of the uncoated control circuits had failed by 200 hours exposure [2].

The evolution of the lower temperature thin film application processes and advances in packaging technology led to the concept for thin film protection of plastic packaged ICs conducted in the Air Force sponsored Reliability Without Hermeticity (Rw/oH) program, (CF33615-90-C-5009) [3]. In this program, Dow Corning was teamed with the advanced packaging group at National Semiconductor to demonstrate improved reliability of die coated with a two-layer coating of silicon oxide and plasma-SiC in plastic packages. The packaging concept is shown in Figure 5.

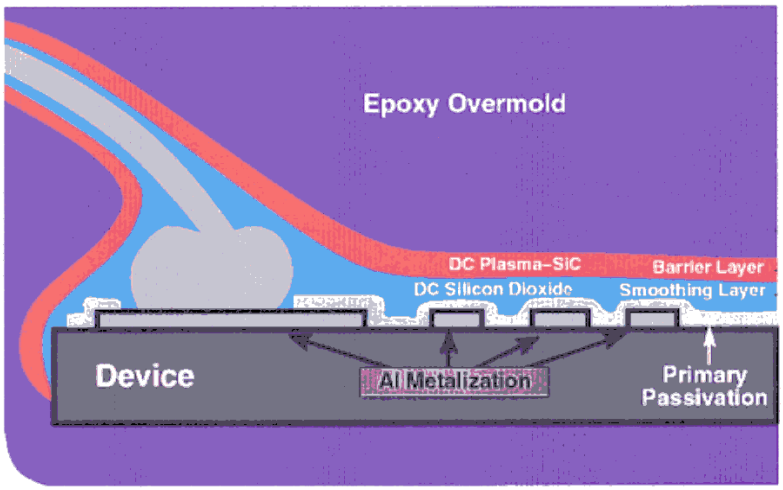


Figure 5. Ceramic/Epoxy IC Packaging Structure for Rw/oH

The program involved the application of the protective coatings after partial leadframe assembly (die attach and wire bonding) but before final plastic encapsulation. Statistical quantities of National's CD4011 CMOS and LM124 op amp devices were assembled, coated and overmolded using National's standard plastic packaging process.

Comparative reliability evaluations, were performed in direct and sequential temperature cycling, autoclave, and HAST exposures. Hermetic packaged die were also included as a control lot. The sequential testing clearly distinguished the long-term reliability of the various packaging systems. The reliability of the Rw/oH devices subjected to HAST (Figure 6) far surpassed that of standard plastic devices and approached that of hermetic package reliability.

Despite the success of the Rw/oH project, it was found that there are inherent limitations involved with the application of additional protective films at the device assembly level. At this stage of production, the IC die left the pristine environment of the semiconductor cleanroom fabrication area and are subject to chemical and particulate surface contamination during dicing, mounting and lead bonding operations. This contamination is difficult to remove and limits the integrity and performance of any subsequent thin film coatings.

Other limitations include the following:

- The restriction to process accessible assembly configurations
- The vulnerability of bare assemblies to possible handling and process damage
- The use of specialized process equipment and unproven manufacturing methods, all of which can contribute to increased cost.

These obstacles can be overcome by integration of the protective coating process with the device wafer fabrication processes.

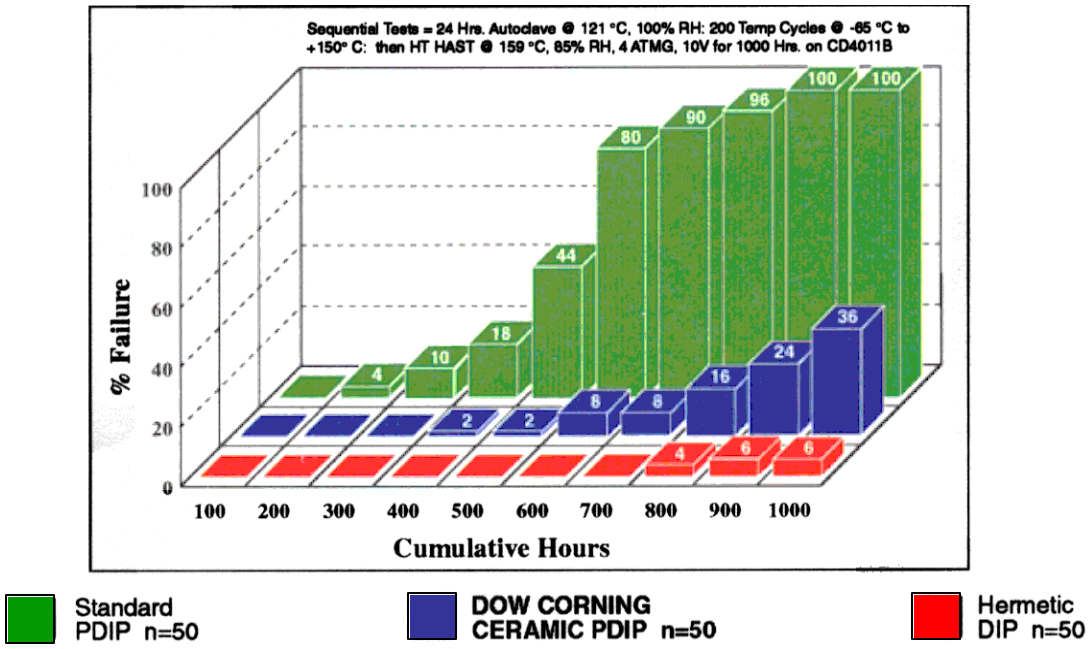


Figure 6. Sequential HAST Test Results for Ceramic-Coated/Plastic Encapsulated CD4011 CMOS Devices

Implementation of the hermetic passivation process at the wafer fabrication stage can yield a highly reliable IC with the versatility to be used in any interconnect configuration. But to achieve this goal, the device contact metallization must be as robust as the dielectric passivation since these areas must be left exposed to the environment. Modern metal diffusion barrier technology has been tailored to meet the process requirements of back-end-of-line IC fabrication. When combined with gold metallization, a stable, noncorroding metallization results. This high reliability metallization can be applied directly over pre-existing aluminum contacts without concerns for failures that would occur from the formation of Au/Al intermetallics. The protective dielectric passivation, when combined with this high reliability electrical contact metallurgy at the wafer level, produces an IC whose surface is equivalently hermetic.

The main issue of consideration is the order in which the two primary processes are used in the ChipSeal scheme: the application of the high reliability metal and the dielectric. There are inherent difficulties with the application of the high reliability metal before the dielectric coatings (referred to as “metal first”):

1. The processing of metal layers first can result in particulate generation that can produce defects in the protective dielectrics applied on top.
2. The application of the high reliability metal over the contact region prior to the dielectric films results in very high steps near the contact edges. Planarization of the steps with the Dow Corning oxide material would be extremely difficult and could lead to cracks in the oxide layer if an extreme thickness is required.
3. The etch process to open the windows has to be controlled in such a way as to stop precisely at the oxide/gold interface. This would require a two-step etch process, a dry etch for the SiC

passivation and a wet etch for the oxide. In a dry etch process, overetch into the gold would lead to gold contamination of the etch chamber, which could be catastrophic to the reliability of other device wafers processed in the same tool.

A small lot of wafers were processed with "metal first" to assess the level of difficulty. Confirmation of the inherent processing issues was obtained. As a result, it was decided that the metal would be applied after the protective dielectric coatings. The structure is shown schematically in Figure 7. This provides a clean surface for deposition of the silicon oxide and carbide films, and since the windows are opened prior to the gold deposition, this circumvents the gold contamination issue. Also, only a single dry etch process is needed to open the windows in the dielectrics, thus reducing cost. The high reliability metals are etched last using wet processes.

3.1 *The ChipSeal Inorganic Sealing Technology*

ChipSeal is an advanced inorganic dielectric passivation deposited from "molecular-designed" silicon materials to specifically meet the present and future passivation and packaging needs of the electronics industry using standard semiconductor process technology [4]. First, a spin-on flowable oxide film is deposited from a carbon-free silica precursor of hydrogen silsesquioxane, which planarizes the surface. Smoothing the surface prevents the formation of defects in the passivation at severe changes in the surface topography. Second, a plasma silicon carbide film is deposited from a single-source, nonpyrophoric, trimethylsilane gas. The SiC material is resistant to chemical etch and moisture adsorption, provides high scratch resistance, and is an excellent thermal expansion match to silicon. These dielectrics are combined with a high reliability noble metal bondpad metallization to produce a more robust IC for advanced packaging applications.

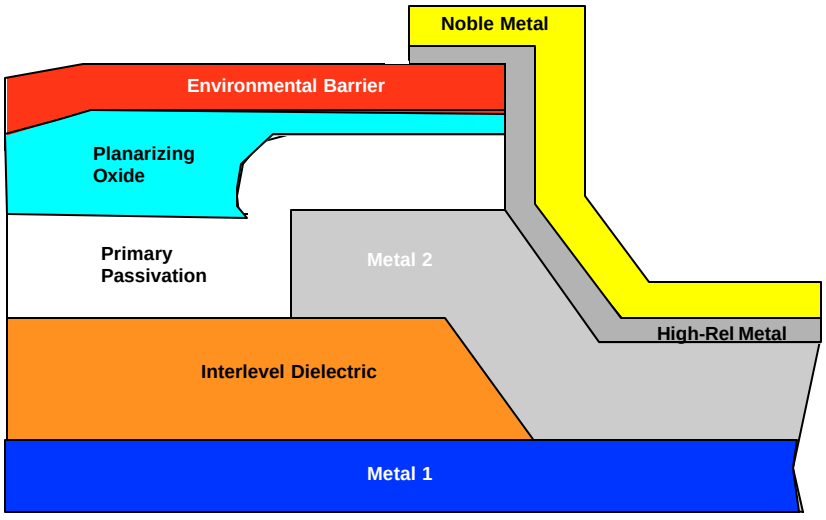


Figure 7. ChipSeal Coating Structure

3.2 *The ChipSeal Program*

With the assistance of the U.S. Air Force Research Laboratory, this program was initiated to demonstrate that the ChipSeal technology could provide hermetic equivalent performance for ICs used in bare die COB, flip-chip, or PEM formats. The goals of the program are as follows:

1. Transfer the Dow Corning (DC) materials and process technology to a third-party processing house.
2. Integrate the ChipSeal passivation with high reliability bondpad metallization technology.
3. Demonstrate process compatibility and reliability on live devices.

The program was organized in two phases: Phase I, technology development and Phase II, technology implementation.

3.2.1 Phase I. Technology Development

The objective of Phase I was to develop the four main supporting technologies and to demonstrate "proof-of-concept" for device compatibility and hermetic equivalence on test devices. The tasks conducted in Phase I were as follows:

1. Transfer and optimize the processes for the ChipSeal passivation coatings to a third-party custom coater.
2. Develop and successfully integrate the high reliability contact metallization.
3. Demonstrate the compatibility and reliability on functioning test devices.
4. Demonstrate the process compatibility with flip-chip interconnect.

3.2.2 Phase II. Technology Implementation

The objective of Phase II was to implement the technology on a variety of production devices to demonstrate its compatibility with commercial processes and to evaluate its applicability to advanced packaging systems. The tasks conducted in Phase II were as follows:

1. Demonstrate process compatibility on commercially produced devices.
2. Process and test ChipSeal on commercial devices in flip-chip format.
3. Process and test ChipSeal in plastic encapsulated devices.

Also, under Dow Corning funding, in collaboration with Rockwell International, Collins Laboratory, MCM integration studies were completed. This effort included KGD and environmental reliability evaluations on ChipSeal processed devices in standard and flip-chip formats, both with and without epoxy encapsulants or underfills.

4. Phase I - ChipSeal Process Development

Two primary processes are used in the ChipSeal Inorganic Sealing Technology: 1) the deposition and patterning of the thin film dielectrics and 2) the deposition and patterning of the high reliability metallization. To achieve hermetic-like reliability, both individual processes, as well as the integration of the two processes, must be developed to form a robust barrier that is stable under severe environmental exposures.

4.1 *Development of Deposition Processes for the ChipSeal Dielectric Passivation*

The ChipSeal dielectric passivation consists of two submicron thick films, a planarizing silicon oxide film and a passivating amorphous hydrogenated silicon carbide film (plasma-SiC). The role of the planarizing film is to enhance the coverage of the primary passivation by filling and sealing any existing surface defects. The source material is a commercially available product, Dow Corning® Flowable Oxide, or FOx®, which is primarily used as an interlayer dielectric (ILD) in the fabrication of semiconductor devices in production today. Dow Corning Z3MS® Trimethylsilane was chosen as the plasma-enhanced chemical vapor deposition (PECVD) precursor gas for the deposition of the SiC films in this program because of its many advantages over other silicon carbide systems. It polymerizes directly to an amorphous hydrogenated SiC in an inert gas plasma without the need for a separate carbon source, it is nonpyrophoric and thus safer and easier to handle than silane-methane systems, it is easily inserted into existing PECVD systems with little modification, and it produces uniform films with low stress. Dow Corning transferred the materials and processes to Sarnoff Corporation, Princeton, NJ, which further refined and customized the process based on its existing equipment and operating procedures.

4.1.1 Silicon Oxide Deposition

The planarizing oxide film is applied by spin coating. The FOx is applied using commercial spin coaters designed specifically for use with liquid oxide precursors. In this effort, a SEMIX spin coater, manufactured by Tazmo (Japan), was used. The coater consists of a spinning region or bowl, and a track, which can pass the coated wafer onto heated plates that are operated in a nitrogen ambient. The parameters used for the SEMIX unit are listed in Volume 2.

FOx is a resinous material based on hydrogen silsesquioxane and consists of silicon, oxygen and hydrogen. The material is dissolved in a hydrocarbon solvent and dispensed onto the spinning wafer in the coating unit. Once applied, the film is heated on a series of hot plates up to 400 °C under N_2 to permit the coating to melt and flow. In this application, the FOx is applied at the end of the IC processing steps. To maintain the greatest circuit reliability, the aluminum in the IC must not be exposed to temperatures exceeding 425 °C. This limits the maximum process temperature for the FOx film. Heating the FOx film induces chemical pyrolysis. Depending on the degree of thermal energy provided, the material will undergo molecular rearrangement, liberate hydrogen and hydride gases and convert to a partially oxidized form ($HSiO_x$). Adjustment of the process conditions can be used to control the amount of rearrangement and conversion to oxide. The degree of conversion determines film properties such as composition, stress and dielectric constant.

During the process development for the ChipSeal application, two methods of FOx conversion were studied. One method involved placing the wafers in a PECVD system and exposing the films to oxygen plasma. This approach has the added benefit that the plasma-SiC film can be applied immediately following the FOx anneal, without breaking vacuum. The alternate method explored a 400 °C anneal in a nitrogen purged ambient using a standard quartz diffusion furnace. This is the method currently being adopted for most of the ILD applications.

Oxygen plasma processing of the FOx was performed in an ASM PECVD system. The process chamber conditions are as shown in Table 2.

Table 2. Process Chamber Conditions

Process Characteristic	**Condition**
Chamber Temperature:	350 °C
Chamber Pressure:	2.0 Torr
Oxygen Flow:	450 sccm
RF Power:	200-300 watts
Process Time:	10-45 minutes

A 300 W, 45 minute exposure resulted in an essentially hydrogen free silicon dioxide film, as determined by the removal of the Si-H bond vibration visible in an IR spectrum of the film. This process caused the film thickness to shrink about 10 percent. Treatments at lower plasma power or less time resulted in films with increasing levels of hydrogen. The 45 min/300 W process was implemented on test wafers that had device topography patterned onto the surface. Following the process, plasma-SiC layers were grown on top of the oxide. The process was repeated three times with no difficulties.

In contrast to the plasma conversion of the FOx, the nitrogen furnace anneal does not completely remove the hydrogen from the film. A 400 °C anneal was examined, the details of this processing are described in Volume 2. A 60 minute anneal cycle results in about 6 percent film shrinkage. Throughout the hot plate stages on the spin coater and the nitrogen anneal, the refractive index of the film did not change appreciably from its value of 1.40.

The planarization properties of FOx films were qualitatively evaluated using SEM analysis of cross-sectioned wafer samples with various surface topography. All samples had plasma-SiC films deposited above the FOx layer as shown in Figure 8. For all conditions examined, no cracking was observed in the FOx layers and the plasma-SiC layer thickness was constant over all features. In some samples, regions of lower density were observed that correlate with the regions on the device surface where the FOx layer reaches maximum thickness. The differences between the furnace anneal and the oxygen plasma anneal are minimal.

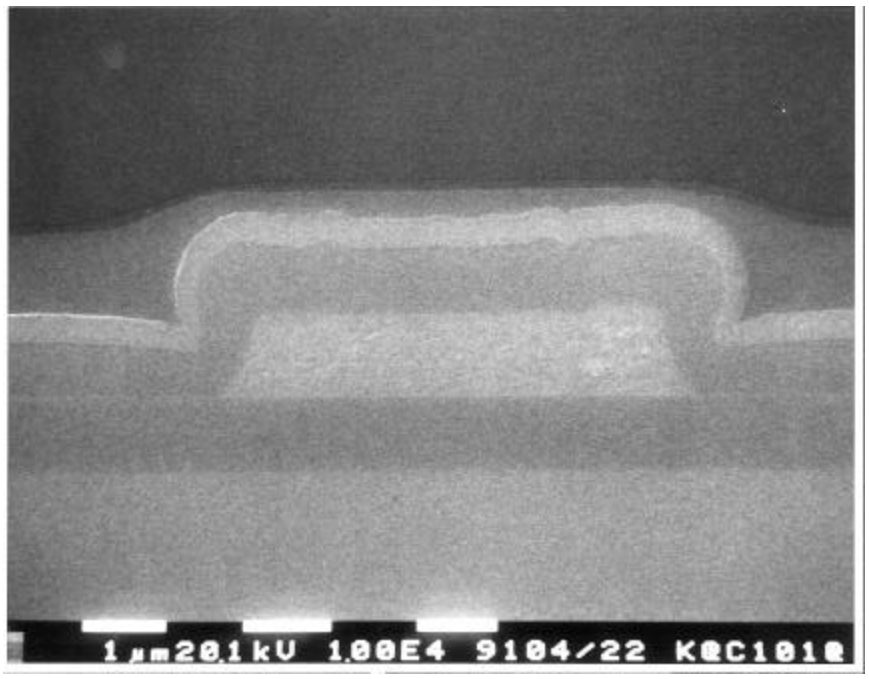


Figure 8. Cross-sectional Photomicrograph of a Device Wafer Illustrating Coverage of the Spin-on FOx Derived Silicon Oxide Film

4.1.2 Silicon Carbide Deposition

Dow Corning's prior SiC plasma deposition experience has been in parallel plate PECVD reactors such as the PlasmaTherm 790 and Applied Materials P5000. For this program, the process and application development efforts relate to the following:

- The transfer of the materials and processes to Sarnoff Corporation for start-up within their 100 mm ASM PECVD tube system.
- The process development and characterization of the films produced.
- The scale-up of the system and process to accommodate 150 mm diameter wafers.

Also included were the evaluations of different carrier gasses as a means to lower process temperatures, and evaluations to determine the feasibility for film growth after insitu FOx cure in the PECVD apparatus.

The existing 100 mm ASM PECVD furnace was modified with a new tube and boat to accommodate 150 mm wafers. The films produced after the modification had equal uniformity and stress to those produced previously. Numerous blank and pattern test wafers, and eventually functional device wafers were produced in the system using the detailed conditions described in Volume 2.

4.2 *Development of Etch Process for the ChipSeal Dielectric Passivation*

4.2.1 Process Approaches

The process steps used to open the bondpad windows in the protective dielectric coatings are a critical element in the ChipSeal process. The plasma-SiC layer is chemically inert and requires a plasma etch process. Care must be taken so that the final process is controllable with respect to the underlying dielectric and metal. Also, the process needs to be simple, cost effective, and compatible with IC manufacturing. The following two approaches were initially considered:

1. Plasma etch of the SiC and a wet etch of the SiO_x.
2. Plasma etch of both the SiC and SiO_x.

A wet etch is of concern because of the potential to undercut at the SiC/ SiO_x interface.

Preliminary etch studies were conducted in a PlasmaTherm A-360 inline etch system using CF_4 or Cl_2 plasma chemistries and in a Tegal 1513 oxide etch reactor using C_2F_6/CHF_3/He gases. Etch rates were first determined on individual SiO_x and SiC films deposited on Si substrates (thickness 0.33 and 0.5 µm respectively) and then on a SiO_x/SiC/Al-1 percent Si sandwich (thickness 0.5/0.33/1.0 µm). Etch rates for the individual films were determined as a function of plasma power and gas pressure. The optimum process conditions were then used to determine the best etch system for developing tapered sidewalls on the openings etched in the SiC/SiO_x multilayer structure on the Al metallized substrate. The relative individual etch rates are shown in Table 3.

Table 3. Comparative Individual Film Etch Rates (Å/min)

Etchant	SiO_x	SiC	Resist
CF_4	575	650	1000
Cl_2	445	1350	2200
C_2F_6/CHF_4	6700		2000

The decision to place the high-rel metallization on top of the ChipSeal SiO_x/SiC structure greatly simplified the entire etch process. This approach eliminates issues related to gold contamination of etch chambers when the barrier metal is applied first. A fluorine-based plasma chemistry was chosen as the prime candidate since it can etch through both the oxide and carbide layers in one step. The fluoride type of etch is also selective to aluminum, thus minimizing the risk of overetch. A chlorine-based chemistry was also evaluated for its selectivity. Overall, this approach reduces the number of process steps, simplifies the process, and reduces the ChipSeal processing cost.

It should be noted that the etched sidewall taper depends strongly on the relative etch rates of the SiO_x and SiC (and photoresist) and can be adjusted by varying the etch chemistry, process power and pressure. Having a low angle uniform taper is important in achieving uniform step coverage of the opening in subsequent metallization steps.

In the multilayer etch studies, the CF_4 etch system produced smooth, uniform, 55 ° tapered wall structure. The sequential Cl_2 - C_2F_6/CHF_3 produced a steeper wall profile for the SiO_x layer and etched the aluminum surface, potentially affecting the reliability of the subsequent metallization layers.

4.2.2 Final Process Selection

The results suggests that the CF_4 process has many advantages over the other processes. The major advantages of using the CF_4 process for etching both SiC and SiO_x layers are listed as follows:

- Tapered wall profiles for both SiC and SiO_x.
- Does not require two separate reactors.
- Noncorrosive gas chemistry.
- Reduced number of process steps.
- Process can tolerate significant overetch since etch rate of Al in CF_4 is extremely low.
- Minimizes wafer handling.
- Does not require very good selectivity between SiC and SiO_x.

It should be noted here that the etchrate for O_2 plasma converted FOx layer (i.e., the SiO_x layer) was ~30 percent lower as compared with the furnace-annealed FOx layer (for which the Si:H peak has almost no reduction after conversion). It should also be noted that alternative processes could also be developed by using CF_4+O_2 gas mixtures. For the process development work reported here, oxygen was not used due to the absence of an additional oxygen gas channel on the PlasmaTherm inline reactor.

However, the effect of adding oxygen to CF_4 was studied in an Anelva 405 reactive ion etch (RIE) batch reactor. A combination of CF_4 and O_2 can also be used for etching the SiC layer. For the small parameter space studied in this experiment, an 8 percent addition of oxygen increased photoresist and SiC etch-rates by approximately 60 percent and 40 percent respectively. Thus, a minute amount of oxygen can be added to CF_4 (as is done in many polysilicon and nitride etch processes) to increase the etchrates of these dielectrics for higher throughput at the cost of having thicker photoresists.

4.2.3 Effect of SiC Deposition Parameters on Etch Rates

It is expected that the properties of deposited SiC films from different fabs will be slightly different because of differences in tools and operating parameters. Etchability of various SiC films with different deposition parameters and stresses were investigated to ensure transferability of the etch process from one fab to another. Deposition parameters, properties and etchrates for various samples used for this study are summarized in Table 4. No significant difference in etchrates was found for these samples and etchrates were within 25 percent of each other for all samples.

The results suggest that the plasma-SiC dry etching is fairly independent of the deposition processes using Dow Corning Z3MS® Trimethylsilane as the precursor gas.

Table 4. Deposition Parameters, Properties and Etchrates of Various SiC Samples

Sample #	Temp °C	Power W	Pressure Torr	Ar flow sccm	He flow sccm	3MS flow sccm	Dep.rate Å/min	Ref. Index n	Stress 10e9 dynes/cm2	Etch-rate Å/min	3-sigma unifor
2-4	400	200	2.0	500	-	63	350	2.48	4.0	914	6.3
1-9	350	200	2.0	500	-	63	437	2.43	2.0	991	7.0
1-12	350	200	2.0	500	-	63	437	2.43	2.0	933	6.4
1-13	300	200	2.0	500	-	63	385	2.38	0.83	1125	6.6
1-16	300	200	2.0	500	-	63	385	2.38	0.83	1121	5.6
2-5	250	200	2.0	500	-	63	523	2.35	1.3	1132	5.3
2-8	250	200	2.0	250	-	63	523	2.35	1.3	1074	5.1
2-17	300	200	1.5	250	750	126	215	2.65	4.0	965	3.2
2-20	300	200	1.5	250	750	126	215	2.65	4.0	884	4.9
1-21	350	200	2.0	500	500	63	500	2.63	3.2	973	7.1
1-24	350	200	2.0	500	500	63	500	2.63	3.2	1035	7.8
2-21	350	300	1.5	500	-	126	900	2.44	0.96	847	5.6
2-24	350	300	1.5	500	-	126	900	2.44	0.96	926	4.4

4.2.4 Feasibility of Transferring the Etch Process to Another Semiconductor Process Tool

It is very important for the success of the ChipSeal technology that the process developed under this task should be easily transferable to other process tools. Initial feasibility of transferring the CF_4 based etch process to another reactor was demonstrated by developing a similar process on the Anelva 405 RIE reactor. This machine is a batch reactor capable of handling 4, 5 and 6-inch wafers. The wafers are placed on a rotating (~5 rpm) RF electrode, which is approximately 50 cm in diameter. Ten 4-inch wafers can be processed in this machine in a single run. A 500W, 50 mTorr condition was selected for this reactor. SiC and SiO_x layers were etched on a metallized substrates. The etched wall profiles achieved with this machine were very similar to those produced in the PlasmaTherm, despite very different reactor configurations. It should be noted here that the process window would be different for different reactor configurations. However, the process window for a specific reactor can be determined easily since the CF_4 gas chemistry is commonly used in the semiconductor fab.

4.2.5 Etch Process Summary

Various etch processes based on fluorine and chlorine plasma chemistries were investigated in PlasmaTherm Inline and Tegal 1513 reactors for etching SiC and SiO_x layers. An etch process using a CF_4 plasma in the PlasmaTherm Inline reactor was selected for etching both SiC and SiO_x layers for the ChipSeal program. This process allows etching of both layers in a single step using noncorrosive gas chemistry and produces tapered sidewall profiles as shown in Figure 9. This process allows up to 45 percent overetch without significantly affecting the taper of the sidewall. Also, the etch process was found to be invariant to the size or alignment of the ChipSeal bondpad window. For window alignments inside, coincident, or outside of the primary passivation window, the process produced sufficient taper to provide good step coverage for the barrier/noble metallization. It was also demonstrated that a residual SiO_x layer could be left on

the bond-pad (extending out a few micron from the SiC-edge) for improving step coverage of barrier/noble metallization. Finally, initial feasibility of transferring this process to another reactor (Anelva 405 batch RIE etcher capable of handling 4, 5 and 6-inches wafers) was demonstrated.

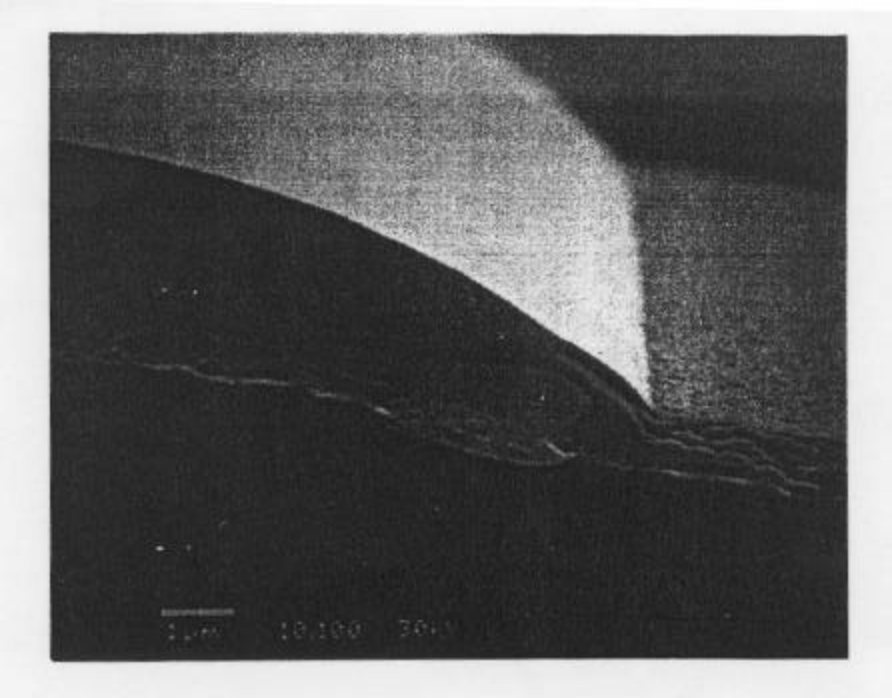


Figure 9. Typical Etched Bondpad Sidewall Profile

The process may need to be further refined if the thickness of these layers were to be changed or the step coverage of barrier and/or noble metallization were poor. The most important factor affecting the taper of the sidewall profile is the photoresist/SiC and photoresist/SiO_x etch rate ratio. An etch rate ratio of 1:1 or greater is desirable for this dielectric stack. The photoresist thickness may need to be adjusted for this etch process to work for various thickness of SiC and FOx layers while allowing some thickness (minimum 2 KÅ) of photoresist to be left on the wafer at the completion of the etch process. It is also advisable to include a presputter etch clean step before deposition of barrier/noble metal deposition to minimize contamination from any unwanted residues from the etch/strip process.

4.3 *Development of a High Reliability Metallization for the ChipSeal Technology*

Since the overall effectiveness of this wafer-level protection technology depends equally on the reliability of the metallization and the plasma-SiC layer, substantial effort was devoted to the selection and development of a multilayer system that could provide the required corrosion protection and compatibility with the existing contact metals. The requirements for any high quality metallization system are that it provides a stable high conductivity, provides good adhesion to adjoining metals, is resistant to intermetallic compound formation and electromigration, is amenable to standard production methods for deposition and patterning, and provides low, stable stress values at deposition and during subsequent process heat treatments. Also, in order to provide environmental protection in the absence of a hermetic enclosure, the

metallization must itself be corrosion resistant. The strategy for such a system is a noble metal over an appropriate barrier metal, which are applied and patterned after application of the ChipSeal passivation coatings (Figure 10). The challenge is in defining the best barrier metal for the system.

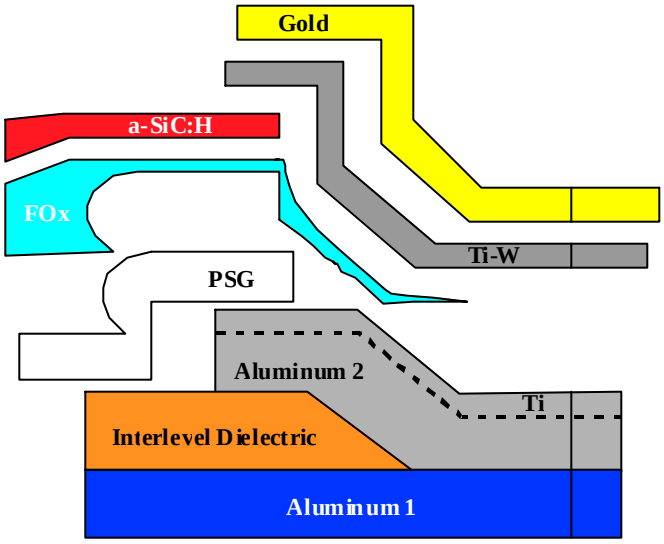


Figure 10. TiW/Au Metallization Structure on Top of ChipSeal Protective Dielectric Coatings

Gold was the immediate choice for the noble metal contact. Gold presents a chemically inert, nondegradable surface to which excellent electrical and mechanical contacts can be made. However, gold does diffuse rapidly into aluminum, placing a greater burden on the barrier metal. Three barrier metal systems were considered and investigated: Ti(20 atomic percent)W, Ti(20 atomic percent)WN, and TiN. The choice of barrier metal was dependent not only on its effectiveness as a diffusion barrier, but also on its compatibility in processing with the other thin film constituents. A decision had been made early in the program to pattern the layers by wet chemical methods in order to minimize cost. Highly specific and selective etchants would be required. TiW is a commonly used barrier in many IC applications and as early as 1978, it was reported to effectively prevent interaction between Al and Au [5]. There are several useful wet etchants available for this material based on Ti or W, so that different process options for patterning are possible here [6]. "Stuffing" nitrogen into TiW results in considerable improvement in barrier properties [5]. Films of Ti (20 percent) WN were deposited, but control of the nitrogen content was problematical and no effective wet etchant is known. The TiN also has good barrier properties [7]. It is prepared by reactive sputtering at many IC facilities and etching by wet or plasma methods is reported. Thus, TiN can also be readily incorporated into IC processes.

Another important reliability consideration is the integrity of the metallization, especially that of the Al and Al alloy conductors, with respect to corrosion. Corrosion may occur during both manufacture and long-term operation. Halide ions introduced in plasma and wet etching may become trapped or absorbed on the constituents of devices and induce corrosion at localized galvanic couples. The relative susceptibility to corrosion was determined by measuring the corrosion potentials of the various couples in the metallization. The corrosion potential is the potential of a corroding surface in an electrolyte relative to a reference electrode measured under open-circuit conditions.

A galvanic table was constructed based on the galvanic couples formed between Au and the three barrier metals and the three barrier metals and the metal 2 conductor, Al-1 percent Si [8]. Unlike "textbook" tables of standard potentials for pure materials, this procedure offers direct intercomparison of the actual metals and alloys used in the microelectronic structures under consideration. The corrosion potential may be affected by film stress, non-equilibrium phases, grain size, and surface texture [8]. The electrolyte employed in the measurement can approximate actual conditions of highly dilute solutions found on devices or concentrations commonly used in environmental or accelerated corrosion tests. Such electrochemical techniques are preferable for the characterization of the corrosion behavior of materials that generally have been measured by accelerated weathering using humidity cabinets, saline sprays, or outdoor exposure of test specimens. As opposed to these methods, electrochemical characterization generates quantitative results and a relative ranking can be established.

4.3.1 Experimental Procedures and Results

4.3.1.1 ***Sample preparation***

Silicon wafers (100 mm in diameter) were coated with blanket metallizations that represent the various ChipSeal metallization schemes proposed. A blanket film of aluminum was followed by one or more layers of barrier metals with and without the gold. The target thickness of the individual metal layers are shown in Table 5.

Table 5. Metallization Thickness

Material	**Thickness (Å)**
Al	10,000
Ti (hillock suppressant)	150
TiN	2000
TiW	2000
TiW-N	2000
Au	5000

All of the Si wafers were coated with 1 µm of Al-1 percent Si and with 150 Å of Ti (for hillock suppression) in a CVC-2800 multitarget sputterup system. The TiN of various thicknesses was also deposited in this system when required. Typical deposition parameters for the CVC-2800 are shown in Table 6.

Table 6. Deposition Parameters for the CVC-2800

Metallization	Power	Pressure	Deposition Rate
Al-1%Si:	4 kW, dc magnetron	10 mTorr Ar	200 Å/min
Ti:	3kW, dc magnetron	10 mTorr Ar	200 Å/min
TiN:	3kW, dc magnetron	10 mTorr, equal parts Ar+N_2	33 Å/min

The TiW, TiW-N, and gold films were sputtered in an Innotec VS-24C system. The VS-24C is a four-target (two dc and two rf powered) sputter-down system. Deposition conditions are shown in Table 7.

Table 7. Deposition Parameters for the VS-24C

Metallization	Power	Pressure	Deposition Rate
Au	500 W, rf	10 mTorr Ar	1250 Å/min
TiW	500 W, rf	10 mTorr Ar	300 Å/min
TiWN	500 W, rf	10 mTorr, 15% N_2, rest Ar	~30 Å/min

For the wafers on which film stress was to be measured, the metallization was deposited directly on Si, since the state of stress of the bare wafers prior to metallization had been determined. For other test samples, deposition was on thermally oxidized Si wafers.

4.3.1.2 ***Corrosion Susceptibility Studies***

Six combinations of the metallization were deposited to yield each of the six galvanic couples as shown in Table 8 and Figure 11. Rather than rely on pinholes to form the galvanic pathway, the top layer of the couples, in each case the more noble and cathodic metal, was patterned with an array of small holes to enhance anodic corrosion and the approach to equilibrium.

Table 8. Test Matrix of Metal Combinations Used for Galvanic Corrosion Studies

	Au/Barrier Couples			Al/Barrier Couples		
Sample No.	1	2	3	4	5	6
Metal						
Au	X	X	X			
TiW	X			X		
TiWN		X			X	
TiN			X			X
Al	X	X	X	X	X	X
Si	X	X	X	X	X	X

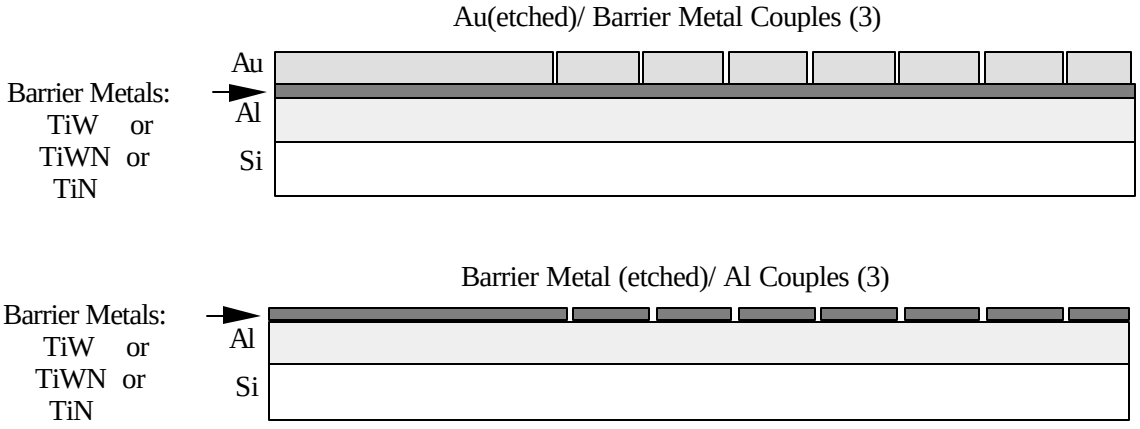


Figure 11. Metallic Couples for the Proposed ChipSeal Metallization

Open circuit potentials were measured with the samples mounted in an EE&G Model K0235 flat cell, Figure 12. The electrolyte was an aqueous 2000 ppm NH_4Cl solution (.0375 N), the same as used by Griffin, et al [8]. A saturated calomel electrode was the reference electrode. Three hundred ml of solution was used per measurement, and it was stirred by two dry nitrogen jets which also removed oxygen from the cell.

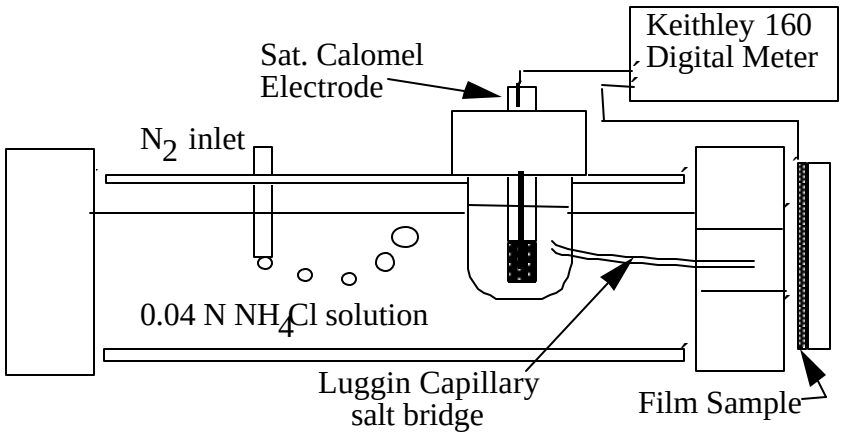


Figure 12. Schematic drawing of a EG&G Flat Sample Electrolytic Cell Showing Placement of Thin Film Samples

Voltages were measured with a Keithley 160 Digital Multimeter. The open circuit potential was monitored immediately upon filling the cell until a stable value was obtained, generally after 3 hours. The potentials reported are with reference to the standard hydrogen electrode and are the average of four or more measurements. Measurements were made on unannealed samples.

A galvanic series of the metallization/barrier-layer couples of possible application in the ChipSeal program and for pure gold and Al-1%Si is listed in Table 9. The series permits the comparison of the open circuit or corrosion potentials of each of the couples and establishes the relative corrosion tendencies.

Table 9. Galvanic Series for Bondpad/Barrier Metal Couples and Barrier Metal/Aluminum Conductor Couples[a]

Film Materials	Corrosion Potential (mv)[b]	% Std Dev
Au	+300[c]	4.8
Au/TiW	+254	3.2
Au/TiN	+177	18
Au/TiWN	+188	8.6
TiWN/Al-1%Si	-414	0.9
TiN/Al-1%Si	-415	0.8
TiW/Al-1%Si	-434	3.1
Al-1%Si/SiO_2/c-Si	-888[c]	2.2

a) All materials were sputtered on thermally oxidized Si wafers except Al samples. The Au/barrier layer couples have an underlying base of Al-1%Si. For the barrier layer/Al-1%Si couples, the Au layer was removed with a KI-I_2 etch.
b) Potentials are referenced to the standard hydrogen electrode.
c) Values of +311 mv for Au and -783 mv for Al-1%Si/ CVD-W were reported by Griffin et al. [8].

All the corrosion potentials of the Au/barrier metal layer couples are positive with respect to the standard hydrogen electrode (defined as 0.0 mv). These potentials are very stable with time. In the case of the three barrier layer/Al couples, the barrier alloys shift the potential of Al in the positive or noble direction.

The potentials of these couples are still negative and indicate that corrosion across the couple will occur at barrier system defects, such as cracks and pinholes in the presence of moisture and electrolyte. All three of the barrier metal systems have roughly the same corrosion susceptibility as shown in Table 10. Thus, the choice of barrier metal is not governed by the corrosion susceptibility alone.

Table 10. Barrier Metal Corrosion Tendencies

Barrier Metal:	TiWN/Al	TiN/Al	TiW/Al
Corrosion:	- 414 mv	- 415 mv	- 434 mv

Corrosion tendency →

The thin Ti layer employed to suppress the formation of Al hillocks is of special importance in such a hermetic metallization. Ordinarily, the presence of hillocks on a metal two conductor is not of concern. However, with a thin (2000-3000 Å) barrier metal system, coverage at the peaks of the hillocks may be poor. Direct Au-to-Al contact may take place at the peaks of the hillocks, with subsequent corrosion and eventual loss of hermeticity. Also, upon annealing or sintering,

Au-Al intermetallic alloys would form, adversely affecting the ability to form strong and reliable gold wire bonds.

4.3.1.3 ***Diffusion Studies***

Estimates of the extent of interdiffusion were made from Auger electron spectrophotometric (AES) measurements at the boundaries of low-angle-lapped samples, and from x-ray diffraction and wire-bond pull-strength tests.

4.3.1.3.1 *AES of Angle-Lapped Surfaces*

Selected annealed samples from the film stress-temperature experiments were angle lapped at less than a degree to provide lateral magnification of the film stack by factors of 65-90. Angle lapping is a rapid process and has the advantage over depth profiling by sputtering in that the depth scale is unambiguously established. Ion mixing, an artifact induced by sputter-depth profiling, is also avoided. Angle lapping also provides a permanent record so that the distribution of species with depth can be reexamined if needed.

The AES was done with a 0.1 µm diameter beam perpendicular to the lapped edge. The depth is known to within ± 75 Å. Table 11 shows several unexpected results from the AES analysis of the metal diffusion study.

Table 11. Diffusion in ChipSeal Metallization - Results of AES from Angle-Lapped Films

Film System	Anneal	Diffusion Results
Au/TiN/Al*/c-Si	As-deposited	Sharp interfaces, no Ti found in Al layer. No Au detected.
Au/TiN/Al*/c-Si	Double annealed at 400°, >8 hr total	Ti diffused to Al/c-Si interface. No movement of Si into Al. No Au detected.
TiW/Al*/c-Si	400 °C, 4 hr	Diffusion of Ti and W into Al, none detected below 1250 Å.
Au/TiWN/Al*/c-Si	400 °C, 4 hr	Only Ti diffusion into Al. No Ti beyond a depth of 4500 Å in Al. No Au detected.

*Al =Ti(150 Å)/Al-1%Si(8 kÅ)

No gold was found on the nitrided films, indicating an almost total absence of interaction between Au and TiN or TiWN. Also, while some of the components of the barrier metal appeared to diffuse through Al, there was no movement of Si up through Al, hence no silicides formed. The amount of Ti that diffused in sample number two could not be qualitatively determined, but XRD showed TiN present as a substantial phase. It should be noted that the anneal times used in the stress studies are considerably longer than would be needed for alloying and other processing steps to which ChipSeal assemblies would be subjected after applying the terminal metallization.

4.3.1.3.2 *X-Ray Diffraction (XRD)*

The XRD method was used in diffusion studies to detect the formation of new intermetallic phases. Selected as-deposited and annealed samples were first examined in situ by x-ray diffractometry. Interpretation of the scans was complicated by a high degree of preferred orientation. The film material was carefully scraped off the Si substrates and Debye-Scherrer x-ray powder patterns were taken. The information on the phases present was obtained from the powder data.

The diffraction results indicate that little change occurred under the stress-temperature anneals of 400 °C for 4 hours other than a sharpening of the diffraction pattern due to a slight increase in crystallite size. Thus even though AES detected Ti diffusion through Al, the amount of cubic TiN in the annealed sample (number two) appeared the same as in the as-deposited (number one). No Al-W or Al-Ti intermetallic phases were seen in the TiW/Al sample, indicating that TiW is an adequate barrier. In the over-annealed sample, on the other hand, extensive new Au-Al compound formation took place, but W appears not to have reacted with Al. Table 12 lists the phases found in selected samples before and after thermal cycling.

Table 12. Diffusion in ChipSeal Metallization - Results of X-Ray Diffraction

Film System	Phases Present
Au/TiN/Al*/c-Si as-dep	Au, Al, and cubic TiN. TiN present to ~5% with < 1000 Å crystallite size.
Au/TiN/Al*/c-Si annealed for > 8 hr	Same as above, narrower lines. TiN still intact.
TiW/Al*/c-Si annealed	Al and W in equal amounts. Lattice constant of W high, a=3.204.
Au/TiWN/Al*/c-Si annealed	Similar to no. 2, but with sharper lines. Cubic phase like TiN may be TiWN.
Au/TiW/Al*/c-Si over- annealed	Sharp diffraction lines. Three phases: Major is cubic Al_2Au, monoclinic AlAu next, and last is bcc W.

*Al= Ti(150Å)/Al-1%Si(8 kÅ)

The compounds of interest as identified by comparison of the observed diffraction patterns to International Centre for Diffraction Data - powder diffraction data are shown in Table 13. The aluminum-gold compounds were formed during the over-anneal. The TiW has the structure of an expanded tungsten lattice, since the alloy is a saturated solution of Ti in W.

Table 13. Phases Detected

Ti 20% - W 80%
Al_2Au
AlAu
TiW

4.3.1.3.3 *Gold Wire-Bond Strength*

The strength of a gold wirebond attachment to an annealed sample is a measure of the effectiveness of the barrier metal and the integrity of the Au film. Gold wirebonds were made on selected as-deposited and annealed samples using 0.001 inch diameter Au wire with a Mech-El Thermosonic Wedge Bonder. The base plate temperature was 120 °C and the transducer was at 70 °C.

Initial gold wirebond tests (Table 14) corroborated the observations made during sample preparation for the AES work. A total inability to bond to Au films deposited on nitrided surfaces verified the lack of adhesion. A very acceptable bond could be made to Au on TiW.

Table 14. Diffusion in ChipSeal Metallization - Initial WireBond Results

Film System	**Bond Strength**	**Type of Failure**
Au/TiN as-dep	-	No adhesion of Au film
Au/TiN annealed	-	No adhesion of Au film
Au/TiW as-dep	20.4 g std dev = 1.4	4 at wire, 1 at bond
Au/TiWN as-dep	-	No adhesion of Au film
Au/TiWN annealed	-	No adhesion of Au film

The lack of adhesion of gold to the nitrided surfaces was unexpected and appeared to preclude further use of TiN, a versatile barrier metal. Experiments to effect a gold-TiN bond through a TiW "glue layer" were carried out. A series of samples to test the effect of different annealing histories on mechanical stress change was prepared, all with structure Au/TiW (400 Å) /TiN (2000 Å)Ti/Al (Table 15). In the first column, the first temperature was the anneal temperature of the TiN prior to deposition of the Au/TiW cap, the second temperature was that during stress measurement. Inspection of the gold overlayer with increasing temperature showed a slight loss of reflectivity of the gold.

Table 15. Diffusion in ChipSeal Metallization - Wirebond Strength with TiW Glue Layer

Sample, °C	Bond Strengths, g	Type of Failure
R1 200 / 200	17.7 std dev: ±1.7	3-wire, 1-ball
R2 200 / 300	18.9 std dev: ± 0.6	3-wire, 1-ball
R4 300 / 300	17.6 std dev: ±2.2	2-wire, 1-ball
R5 300 / 400	17.7 std dev: ±3.6	2-wire, 2-ball

The TiW is seen to function as an effective glue layer for gold on TiN. The effect of the increased temperature does not significantly diminish the bond strength, except perhaps to increase the scatter. The Au layers are intact, and good gold bonding took place.

4.3.2 High-Rel Metallization Etch Process Studies

Etch rates were determined on samples patterned using standard IC methods. The gold was etched with a solution of 2.5 grams of I_2 + 100 grams of KI in 1 liter of water. The etch used for TiW is a mixture of two parts of EDTA solution (2.3 g of ethylene diamine tetraacetic acid (EDTA) + 4.2 ml of NH_4OH in 100 ml of water) and one part hydrogen peroxide (H_2O_2). Thicknesses after etching were determined with a Sloan Dektak Model IIA Profilometer.

The gold films were etched satisfactorily with the KI-I_2 etch at a rate of 1000 Å/min. A drawback of this etchant is its opacity, so that visible clues to the extent of gold removal are not possible. From an environmental standpoint, however, it is very much better than cyanide-based etchants.

An initial choice for the barrier layer was TiN. However, a glue layer of TiW was required between this barrier metal and the Au bondpad. TiW and TiN dissolve in many of the same etchants, but TiW etches more rapidly than TiN, by orders of magnitude in some cases. Extensive undercutting of the thin TiW glue layer occurred in attempts to pattern the underlying TiN, resulting in lifting and loss of the Au bondpads and other fine structures. On the other hand, TiW barrier layers were patterned with the EDTA-H_2O_2 etchant and were removed at a rate of 545 Å/min, Figure 13. This is a selective etch for TiW. Au is not attacked and Al-1 percent Si is etched at a rate 20 times slower.

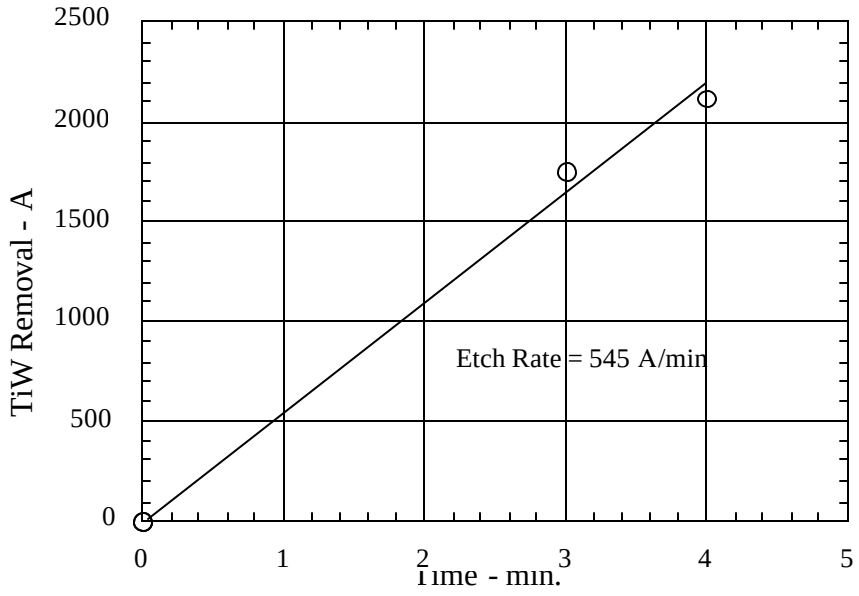


Figure 13. Etch rate of TiW Film in EDTA-H_2O_2 Etch

4.3.2.1 ***Stress Measurement***

Stress measurements were conducted on the barrier and noble metallizations using a Tencor P1 Long Scan Profiler to measure wafer curvature before and after film deposition. A Tencor FleXus 2320 Profiler was used to measure dynamic stress changes as a function of temperature. The temperature treatments performed during the stress measurements simulated the thermal cycling and annealing processes typically used within the fabrication process and was used in this study to assess any adverse impact to the barrier metal system.

4.3.2.2 ***Stress Results***

The as-deposited stresses are shown in Table 16.

Table 16. As-Deposited Stress Rates for Various Films

Film	Stress MPa	Stress Direction
Al/Ti	40	Tensile
Al/Ti/TiN	40	Tensile
Al/Ti/TiW	100	Tensile
Al/Ti/TiW-N	70-80	Tensile
Al/Ti/TiN/Au	70	Tensile
Al/Ti/TiW/Au	110	Tensile

Both the TiN and TiW systems exhibited tensile character with slightly higher stress for the TiW system. The most interesting feature is that when gold is deposited over a generic barrier with

the empirical formula TiW_XN_{1-X}, the film stress increases as x increases, i.e., the gold stress is highest on the TiW and lowest on the TiN. This implies that the structure and modulus of the gold are sensitive to the substrate surface, which may ultimately impact its reliability performance.

The analysis of film stress as a function of temperature was conducted on the various metal configurations. The change in wafer curvature was monitored as samples were exposed to temperatures of 100, 200, 300, and 400 °C in a nitrogen atmosphere. The objective is to determine the changes that might occur in the multilayer films during subsequent ChipSeal processing steps, including possible thermally induced metal interdiffusion.

The aluminum films showed plastic deformation at as low as 100 °C. Successive exposures to 400 °C produced increased tensile stress consistent with densification and increased modulus. A variety of heating rates were investigated (a 4 °C/min ramp, instantaneous, and successive steps to 400 °C). The change in stress (+40 to +60 MPa) was nearly independent of the rate but did increase slightly with the amount of time at 400 °C.

Samples of Al/Ti/TiN and Al/Ti/TiW with and without Au caps were also examined. For the uncapped samples, the stress versus temperature measurements indicate that annealing causes the stress in both the TiN and TiW films to become more tensile, although the change is much smaller in the TiW. The shape of the Al/Ti and Al/Ti/TiN curves are very similar up to 400 °C, indicating minimal mixing or diffusion between the layers. The shape of the curve for the Al/Ti/TiW system was quite different, indicating a likely interdiffusion. Aluminum was evident on the surface of a 400 °C annealed sample.

For the Au capped samples, by 300 °C, the gold layer on the TiN showed severe spallation, whereas the gold on the TiW appeared unaffected until 400°C, where it was apparent that the gold started to dissolve into the underlying metal. Thus, although starting out with a lower initial stress, the TiN system showed lower thermal stability. As the Al/TiN sample was heated and cooled, it exhibited a larger stress hysteresis compared to the Al/TiW with the stress becoming more tensile. It appears that residual nitrogen is trapped in the TiN film during sputter deposition and can evolve during subsequent thermal cycles. This leads to relaxation of the film, an increase in tensile stress, and the spallation of the gold.

For the TiW-N films, the initial stress was intermediate between that of the TiN and TiW -- higher than the TiN but lower than the TiW. Annealing also causes the stress in the TiW-N to become increasingly tensile. Like the TiW alone, the shape of the stress/temperature curve is much different than that of the Al/Ti curve indicating that there is likely to be some diffusion of Ti into the aluminum, although, after a 400 °C anneal, the appearance of the film is unchanged. These results suggest that the TiN would be the best film to prevent aluminum from diffusing to the gold interface.

As indicated previously, gold was observed to spall from the Au capped TiN samples at 300 °C. Further analyses of the stress/temperature data indicated that the failure could have occurred at an even lower temperature. Since it is believed that the spallation was the result of outgassing of the TiN, an additional experiment was conducted wherein a Al/Ti/TiN sample was coated with 5000 Å of Au after a 400 °C anneal. The repeated stress/temperature measurements indicated excellent stability and no change in the appearance of the gold film.

4.4 *Metallization Conclusions*

A literature review and multiple studies completed as a part of this technical effort, clearly shows a substantial improvement in Au-Al intermetallic barrier properties when using a nitride moiety in the metallization stack over the "industry standard" TiW layer. However, process technology has not been developed sufficiently to control wafer to wafer and lot to lot variations as well as its' integration into a gold metallization stack without substantially increasing cost. Therefore, the metallization stack shown below was chosen for the ChipSeal Hermetic Coating structure..

Existing Metallization	ChipSeal Metallization
Al-1%Si (10k Å)	Ti (0.3k Å) / TiW (2k Å) / Au (5k Å)

The choices made in selecting this metallization, to provide a platform for a hermetic seal, were based on the corrosion, diffusion and etching studies described. A double level of protection is offered to the metal two aluminum conductors by the TiW barrier and the Au, in the absence of coincident pinholes and cracks in both protective films. The TiW / TiN stack is a good barrier system, surviving 4-hour, 400 °C anneals, but such temperature / time excursions are well beyond the requirements for electronic assemblies. Also, this TiW / TiN stack is difficult to pattern TiW performs as an effective barrier for up to 1½ hour anneals. This also exceeds the thermal stress range of ChipSeal. The adaptability of TiW to a variety of processes, the excellent adhesion of gold to it, and the high quality of the resulting gold wire bonds make TiW the logical choice for the ChipSeal metallization.

Process tables delineating the formation of the barrier metal-gold bondpad system are tabulated in Tables 17 and 18.

Table 17. Barrier Metal Deposition Process Target Specifications

Description	**Specification**
Metal Target Purity - TiW	99.95%
Metal Target Composition	20 atom % Ti 80 atom % W
Sputter System	Innotec VS-24C
Power (rf)	500 W
Barrier Metal Thickness	2000 Å
Deposition Rate	300 Å/min
Etchant	EDTA-H_2O_2
Etch Rate	545 Å/min

Table 18. Noble Metal Deposition Process Target Specifications

Description	Specification
Metal Target Purity - Au	99.99%
Sputter System	Innotec VS-24C
Power (rf)	500 W
Noble Metal Thickness	5000 Å
Deposition Rate	1250 Å/min
Etchant	KI-I_2
Etch Rate	1000 Å/min

The use of Ti to suppress hillocks in the Al film is strongly encouraged. Coverage of the barrier metal at hillock peaks is generally inadequate. The absence of hillocks will eliminate a major source of weak spots in the barrier layer.

5. Application of ChipSeal Hermetic Coatings to Operational ICs

An ideal test vehicle to assess the feasibility of the ChipSeal technology is one that demonstrates the effectiveness of the coating and is a representative circuit technology that is used by DoD and its suppliers in a wide variety of applications. The use of an existing test vehicle, with successful implementation of the ChipSeal coatings, should demonstrate the commercial and military potential of the technology. The Sarnoff Corporation has developed a 1.5 µm, BiCMOS double-level metal, gate array technology that provides form, fit, and functional emulation of old obsolete integrated circuits. Over two-dozen different types of these general emulation microcircuits (GEM) devices have been manufactured [9].

Sarnoff has been fabricating GEM devices for several years, with well-defined procedures established for testing the functionality and performance of the devices at both the wafer and packaged die level. The standard GEM reliability qualification is performed using MIL-STD-883 procedures. This background enables the evaluations to be sensitive to any changes produced by the ChipSeal process and materials. In addition, wafer acceptance test (WAT) keys are fabricated on the GEM wafers to provide an enhanced capability to test the effects of process/parametric variations on device performance.

5.1 *Manufacture of BiCMOS Device Wafers with ChipSeal Protection*

5.1.1 GEM Process Revisions

The GEM process produces customized silicon BiCMOS devices using gate array technology and a double-level metal (DLM) personalization process. For this program, two circuit types, a 2505 multiplier and a 8205 decoder, were made. For ChipSeal wafers the only change in the GEM process is the metal-II deposition and the bondpad etch. A 300 Å cap of Ti is added to the 10k Å of Al-1 percent Si to prevent hillock formation during the deposition of the phosphorosilicate glass (PSG) overcoat. A dry bondpad etch is used to minimize Ti loss during etch. Hillock reduction promotes the uniform deposition of the barrier metal and prevents thin spots in the TiW layer, which protects the Al metallization from the top-level gold metal. Fourteen device wafers were produced for this program; four wafers were GEM control wafers and ten wafers went into ChipSeal processing.

5.1.2 Final ChipSeal Process

Two sub lots of wafers, each containing five wafers, were run through the ChipSeal process to obtain the GEM parts needed for the reliability test program. One sub lot was run through the full ChipSeal process and another was run without the FOx planarization layer applied. The process split was used to assess the roles that individual ChipSeal dielectrics provided and the process flow is shown schematically in the Figure 14.

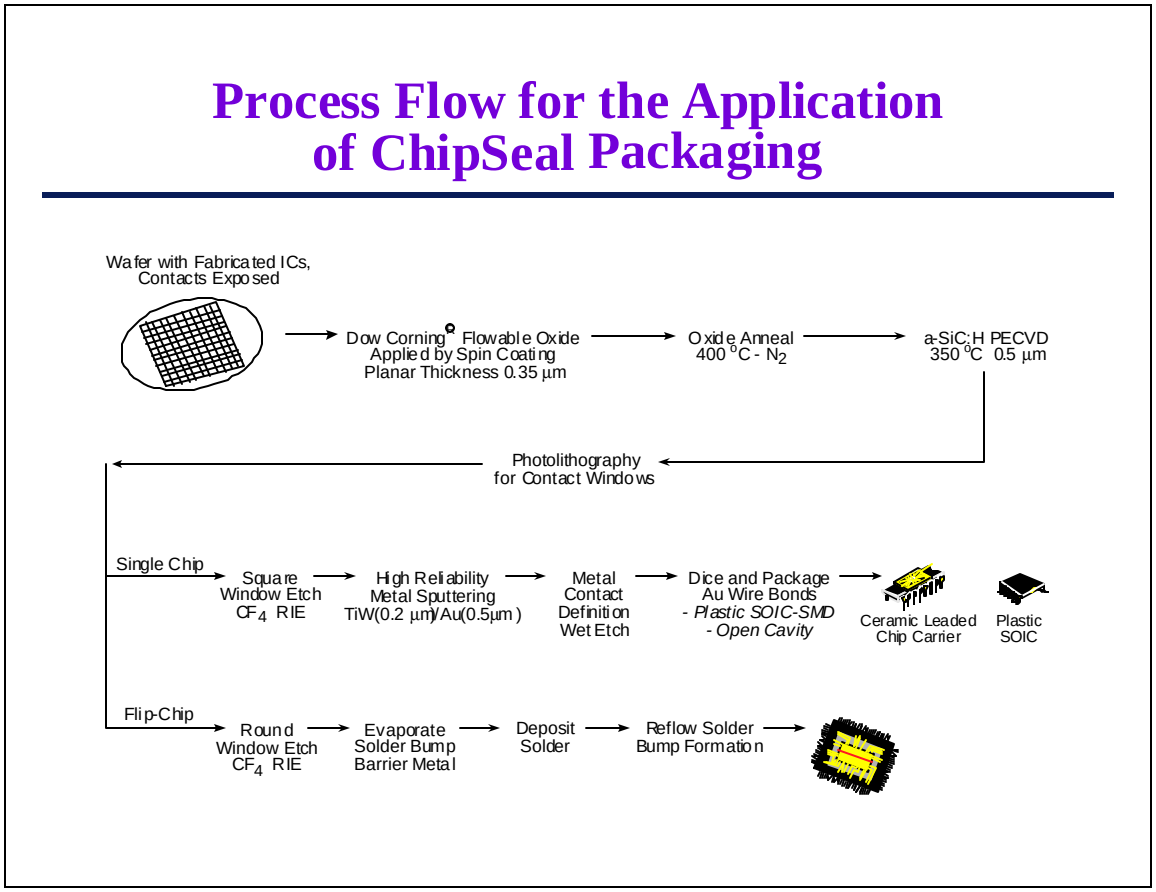


Figure 14. ChipSeal Process Flow for Standard or Flip-Chip Packaging

The ChipSeal process consists of the following steps and conditions:

1. Apply FOx coating.

   FOx coating is applied on a SEMIX coater at a spin speed of 3000 rpm and produces a thickness of 3500 Å after bake. The hotplate bake settings are 125, 200, and 325 °C for 60 seconds.

2. Cure FOx coating.

   The cure is done in a nitrogen ambient at 400 °C for 15 minutes with 20-minute push-pull cycles (~1 hour).

3. Deposit Silicon Carbide.

   This deposition is done in an ASM, plasma-enhanced deposition tube at 350 °C, 2.0 Torr, and 200 watts Rf power at 450 kHz. The gas flows are 63 sccm trimethylsilane and 500 sccm argon. The deposition rate is nominally 440 Å/minute.

4. Bondpad Opening Photolithography.

   The resist application is done using OFPR 800, 70 cps resist @ 2.0 µm thick, and exposed using the normal bondpad mask and development process.

5. Etch SiC/FOx.
   The Anelva batch parallel-plate etcher is used with a CF_4, 60 sccm flow rate at 500 W power and 0.050 Torr pressure. The etch time is approximately 30 minutes.

6. Post Etch Resist Strip.
   A Branson barrel etcher is used for 90 minutes in oxygen plasma.

7. Thin Film Metallization.
   The thin film metal depositions are done sequentially. A 50 second argon sputter preclean is followed by a 2.5 kÅ TiW deposition and then a 5.0 kÅ Au deposition.

8. Bond pad Photolithography.
   A 200 °C oven bake of the metallization stack is done prior to resist application. The OFPR 800, 70 cps resist at a 2.0 µm thickness is applied by spin coating, exposure using a reverse-tone mask that is biased up 17 µm per side and developed.

9. Wet Etch for Gold.
   An iodine/KI room temperature etch is done for approximately 5 minutes.

10. Wet Etch for TiW.
    An EDTA/NH_4OH/H_2O_2 room temperature etch is done for approximately 7 minutes.

11. Resist Strip.
    A Branson barrel etcher is used for 90 minutes in oxygen plasma.

12. Contact Metallization Anneal.
    A 350 °C anneal for 15 minutes in a nitrogen ambient is used to minimize contact resistance.

Figure 15 displays a top view of optical micrographs of GEM after the ChipSeal process. The Au/TiW thin film metal covers the Al bondpads. The barrier metal overlaps the opening in the PSG overcoat by 17 µm per side. The large overlap is present to ensure that undercutting by wet chemical gold and TiW etches do not reach the Al metallization. Figure 16 shows SEM cross-sections of the barrier metal around the bondpad after the TiW wet etch. The photoresist is still on the wafer. Note that the TiW etch undercuts the gold slightly. The gold etch undercut of the resist is 5 to 10 µm, while the TiW etch undercut of the gold is 2 to 4 µm.

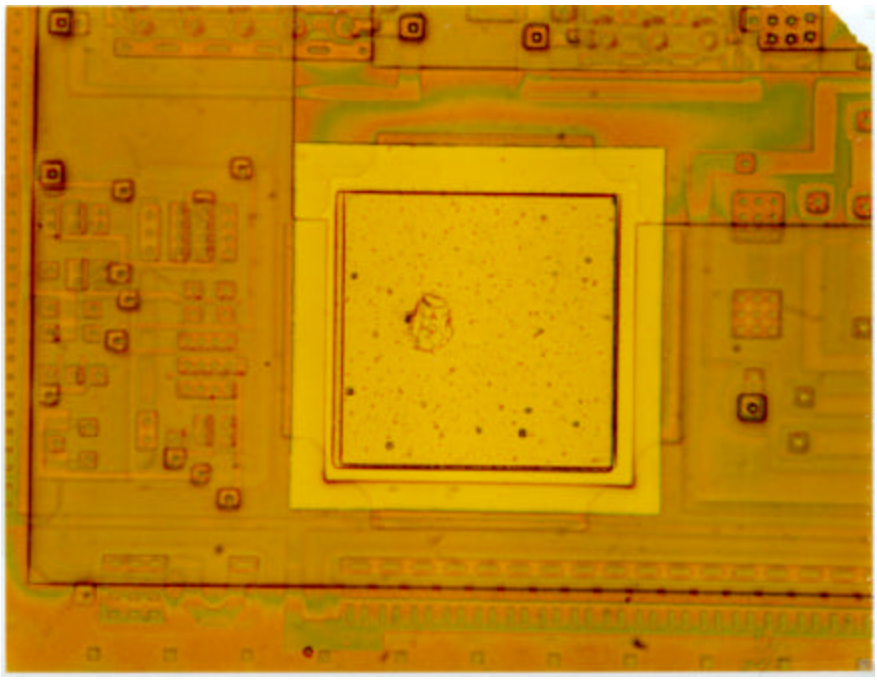


Figure 15. Optical Micrograph of GEM Device after ChipSeal Processing (top view)

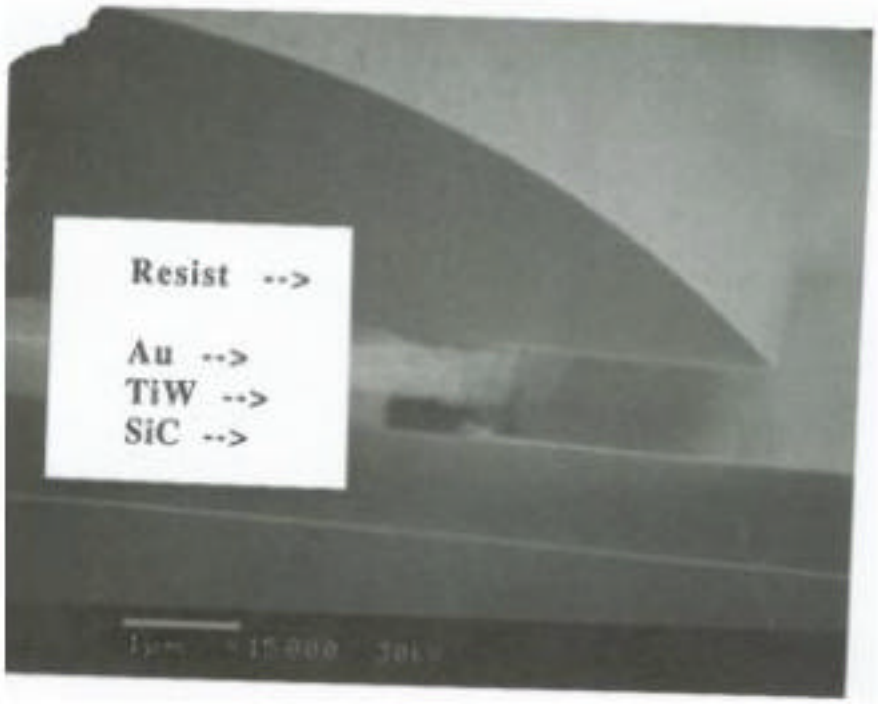


Figure 16. SEM Cross-Section of Bondpad Barrier Metal after TiW Etch

5.2 *Circuit Testing and Process Results*

There is a potential issue of the effects of probe marks on the bondpads of wafers processed with ChipSeal. Probe marks on die probed prior to ChipSeal processing may compromise the coverage of the barrier metallization. Probe of the die after metallization could compromise the integrity of the barrier metal if the gold is penetrated and the underlying TiW or Al is exposed. Microscopic inspection of probed ChipSeal devices did not reveal any obvious exposure of the underlying aluminum metal. However, the potential for exposing the underlying metals still may be possible. Therefore, probed devices will not be used in subsequent packaging and reliability testing. Table 19 lists the ChipSeal wafers, the number of good circuits, and the percent yield after the ChipSeal process as measured at wafer probe.

Table 19. ChipSeal Device Yields

		Control Wafers (No ChipSeal)				
Wafer #	Circuit	Yield	%	Circuit	Yield	%
1	8205	160/192	83	2505	191/224	85
10	8205	151/192	79	2505	146/224	65
12	8205	162/192	84	2505	194/224	87
16	8205	145/192	76	2505	186/224	83
Totals		**618**	**80**		**717**	**80**

		Full ChipSeal Wafers				
Wafer #	Circuit	Yield	%	Circuit	Yield	%
2	8205	114/150	76	2505	151/192	79
3	8205	166/192	87	2505	188/224	84
6	8205	99/150	66	2505	154/192	80
8	8205	161/192	84	2505	162/224	72
9	8205	141/192	73	2505	183/224	82
Totals		**681**	**78**		**838**	**79**

		Partial ChipSeal Wafers (no FOx)				
Wafer #	Circuit	Yield	%	Circuit	Yield	%
11	8205	140/192	73	2505	124/192	65
13	8205	169/192	88	2505	161/192	84
17	8205	131/192	68	2505	130/192	68
18	8205	163/192	85	2505	168/192	88
19	8205	157/192	82	2505	141/192	73
Totals		**760**	**79**		**724**	**75**

5.3 *Technical/Process Issues*

1. Thin Film Metallization - A number of processing issues remain concerning the barrier metal system. These issues should be addressed as part of the Phase II tasks. The effect of probe marks on the barrier metal integrity needs more study. For these initial studies all die probed prior to ChipSeal application were not used, so that there was no possibility of subsequent defective barrier metal depositions. Whether this precaution is of real concern or whether improved barrier metal systems can overcome possible problems should be investigated.

2. Contact Resistance - A series resistance was encountered after applying the barrier metal. A 350 °C anneal in N_2 resolved this issue. The origin of this resistance needs to be determined. The information will be needed to determine the optimum anneal cycle for the barrier metal.

3. Etch Undercut of the Metallization - The TiW wet etch undercuts the gold to some degree. This undercut could reduce the adhesion at the Au to TiW interface by selective attack of this interface by the etchants. Annealing the barrier metals prior to etching or etchant composition changes should be investigated to determine the effect of annealing on the amount of undercut.

4. Metallization Stack - TiW will work if processed correctly but the process window may be improved through the use of TiW-N. This would require improved etch processes or contact patterning processes to minimize undercoat and damage to the dielectric passivation.

5. Metallization Thickness Threshold - Thicker TiW films and TiN films are possible ways of providing more robust barrier metal protection. All wafers were probed after Au deposition. The probe marks on the Au metal do not appear to penetrate the barrier metal, but studies of their effect on barrier metal integrity are needed.

6. Edge Effect of the Metallization - The process used to deposit and pattern the metallization over the bondpad region exposes the edge of the barrier layer to moisture and corrosive ions. Methods to completely seal the barrier layer would include either an additional mask step or the use of electroless gold plating. An investigation into either technique could further improve the integrity of the barrier metallization.

5.3.1 Wafer-Level Reliability Tests

WAT keys fabricated with the GEM wafers were used to perform wafer-level reliability tests and to provide early indications of the reliability of devices processed with ChipSeal coatings. The GEM WAT keys contain large area capacitors with thin gate oxides that can be used for capacitance voltage/capacitance voltage bias test (CV/CVBT) on wafers fabricated with and without the ChipSealcoatings. The presence of the test structures and existing test programs provides an enhanced capability to evaluate the effects of ChipSeal process parameter variations on device/circuit performance.

5.3.1.1 ***Wafer-Level CVBT Tests for Alkaline Contamination***

The effectiveness of the ChipSeal coating, with or without the FOx film, against alkaline ion contamination was investigated by measuring flat-band voltage shifts in CVBT curves in test

capacitors before and after salt fog treatment. Capacitors from various test wafers were measured for possible CVBT shifts before the salt fog treatment to ensure that there was no alkaline ion contamination in the wafers to begin with, which could render any subsequent CVBT shifts observed after salt fog difficult to interpret. The CVBT were measured after applying a –10 V bias on the gate for 30 minutes at 280 °C and cooling the wafer to room temperature with the –10 V bias applied to the gate. The –10 V bias on the gate is provided to facilitate lateral or surface alkaline ion migration towards the capacitor. This was followed by a +10 V bias on the gate at 280 °C for 5 minutes to drive any alkaline ions toward the silicon/oxide interface to affect a larger flat-band voltage shift due to the positive alkaline ions, if any. As expected, no CVBT shifts were observed in all starting samples prior to the salt fog treatment, indicating that there was no alkaline contamination during both the normal GEM fabrication process and the ChipSeal process.

After the salt fog treatment, CVBT measurements were repeated on all test samples, which included the control GEM, ChipSeal-GEM and NoFOx-GEM wafers. No significant (<0.3 V) flat-band voltage shifts were detected after negative and positive gate bias at 280 °C. Thus, based on CVBT measurements on large area polysilicon capacitors, we conclude that no significant amount of alkaline ions from the salt fog treatment managed to migrate to the thin oxide layers of the capacitors, even in the standard GEM samples which were passivated with 6000 Å of PSG glass only. The experiment was not able to prove the additional effectiveness of ChipSeal against alkaline contamination.

In an effort to find a more sensitive test vehicle, N-channel metal oxide semiconductor (NMOS) threshold voltages as well as subthreshold current-voltage characteristics of individual test transistors in the WAT keys were measured on the standard GEM samples before and after salt fog treatments, and any shifts in threshold voltages were carefully monitored before and after applying a –10 V gate bias at 280 °C with the source, drain and substrate tied to ground. As before, there were no significant negative shifts of the NMOS threshold voltages on all standard GEM samples, indicating no significant ingress of alkaline ions from the salt fog treatments. These measurements were again repeated after subjecting the standard GEM samples to 350 °C for 8 hours on a hot plate, and, as before, no significant shifts were observable in the NMOS threshold voltages. Thus, no significant amount of alkaline ions from the salt fog treatment managed to migrate to the thin oxide layers of the transistors, even in the standard GEM samples. Thus it was concluded that these wafer level reliability experiments are not sufficiently discriminating to the effectiveness of ChipSeal against contamination incurred by the salt fog treatment.

6. Packaging and Reliability Testing - Wire Bond Configurations

A broad and diverse number of package types are available for microelectronics. Based on the input from semiconductor manufacturing technology (Sematech) member companies, the use of existing, high volume, surface mount type, plastic packages were chosen for this program. The use of an existing package type, with successful implementation of the ChipSeal coatings, should provide a direct correlation to many comparable devices manufactured by commercial semiconductor companies.

In addition, a combination of military and JEDEC specifications were used for screening and reliability testing. The purpose of using JEDEC specifications was to ensure the use of standard reliability tests, endorsed by commercial semiconductor companies, was completed. The use of military specifications allowed for severe reliability tests that would differentiate device performance in adverse conditions.

6.1 *Packaging*

The overall packaging and test flow strategy for the ChipSeal live device demonstration is shown in Figures 17-19. The two types of GEM devices were processed with three test configurations for the wire bond interconnect evaluations:

Standard	=	PSG passivation with Al bondpads
ChipSeal	=	SiO_x/plasma-SiC passivation with high reliability metal bondpads.
NoFOx	=	Plasma-SiC passivation only with high reliability metal bondpads.

After initial wafer level testing, the wafers were diced and subdivided for the various packaging configurations to be tested. One group was packaged using Sumitumo 6300H plastic overmolding compound to produce 95 mil thick, 300 mil wide SOIC. A second group was packaged in ceramic side-brazed, dual inline packages (D-packages) without lids to simulate an MCM bare die assembly. A silver filled polyimide die attach was used and all die interconnects were made with 1.2 mil diameter gold wire. The third group of standard die was hermetically packaged as the control group. These used a eutectic die attach and aluminum wire bonds. The hermetic packages received both gross and fine leak tests after assembly. This breakdown is shown in Figure 18. All packaging was performed at Norsk Engineering, San Jose, CA.

Table 20 and 21 show the initial functional test results for both device types by package style and processing. Subgrouping by wafer lot number is also provided. The data reported is the number of functional failures over the quantity tested (number failed/total). This is the first test data for the packaged devices. Discounting the assembly errors, the final packaging yields are shown in Table 23 for each device type and configuration. The results indicate that the ChipSeal process is compatible with standard interconnect and packaging configurations.

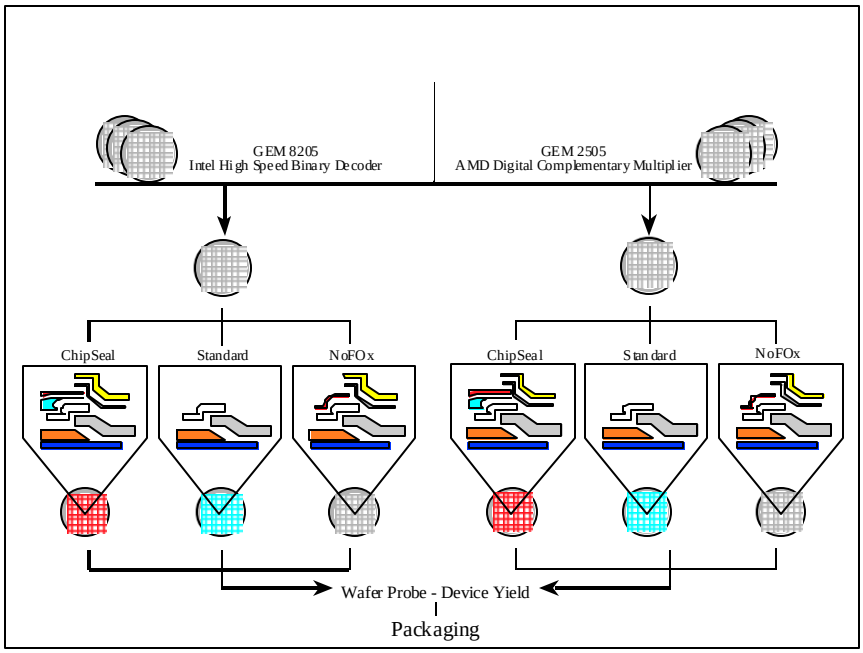


Figure 17. ChipSeal Process Design of Experiment (DOE)

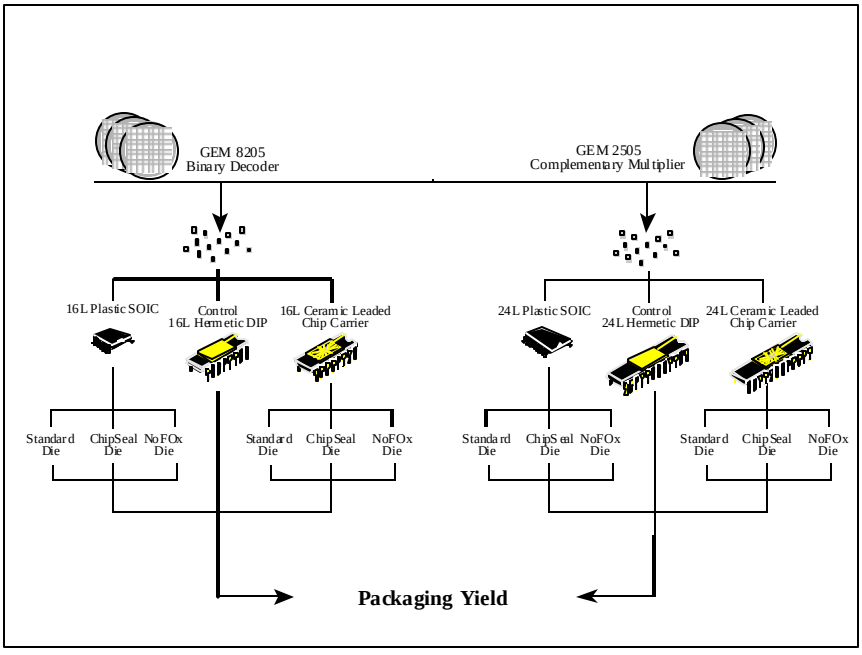


Figure 18. ChipSeal Packaging DOE

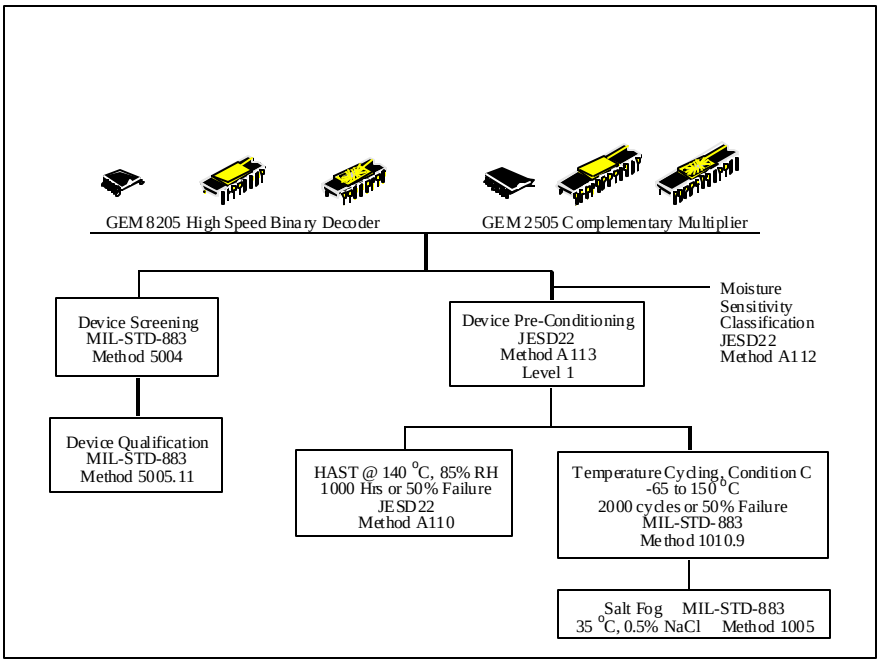


Figure 19. ChipSeal Reliability Testing DOE

Table 20. GEM 16-Lead Device Yields by Package Type and Processing

GEM 8205 16 lead Device						
Package Type	**Standard**		**ChipSeal**		**NoFOx**	
	Wafer #	Yield	Wafer #	Yield	Wafer #	Yield
D-Pak	3A1	3/27	3A2	2/24	3C11	0/21
	3B10	0/26	3A3	0/29	3C13	2/20
	3B12	0/25	3A6	1/19	3C18	0/21
	E16	1/26	3A8	1/24	3C19	0/45
			3A9	0/15		
TOTAL		**4/104**		**4/111**		**2/107**
Hermetic	3A1	1/37				
	3B10	0/19				
	3B12	0/18				
	E16	0/24				
TOTAL		**1/98**				
SOIC	3A1	3/21	3A2	4/11	3C11	0/17
	3B10	2/29	3A3	12/12	3C13	2/27
	3B12	2/29	3A6	33/33	3C18	0/29
	E16	3/21	3A8	2/34	3C19	1/45
			3A9	30/30		
TOTAL		**10/100**		**81/120**		**3/118**

Table 21. GEM 24-Lead Device Yields by Package Type and Processing

GEM 2505 24 lead Device						
Package Type	**Standard**		**ChipSeal**		**NoFOx**	
	Wafer #	Yield	Wafer #	Yield	Wafer #	Yield
D-Pak	3A1	3/26	3A2	0/16	3C11	1/26
	3B10	0/26	3A3	0/23	3C13	0/22
	3B12	1/26	3A6	3/23	3C18	0/27
	E16	1/26	3A8	1/30	3C19	0/34
			3A9	0/25		
TOTAL		**4/104**		**4/117**		**1/109**
Hermetic	3A1	0/21				
	3B10	0/32				
	3B12	0/16				
	E16	0/27				
TOTAL		**0/96**				
SOIC	3A1	2/25	3A2	0/31	3C11	0/10
	3B10	2/33	3A3	--/--	3C13	0/40
	3B12	1/21	3A6	19/30	3C18	0/40
	E16	1/19	3A8	0/30	3C19	1/29
			3A9	30/30		
TOTAL		**6/98**		**49/121**		**1/119**

Table 22. Compiled Packaging Yields by Device Type and Assembly Configuration

GEM 8205, High Speed Binary Decoder			
Test Configuration	Quantity Tested	Quantity Failed	% Yield
Hermetic Controls	170	1	99.4
Standard SOIC	235	36	84.7
ChipSeal SOIC	236	10	96.2
NoFOx SOIC	278	4	98.6
Standard DIP	104	4	96.2
ChipSeal DIP	271	5	98.2
NoFOx DIP	275	4	98.6

Gem 2505, Complement Multiplier			
Test Configuration	Quantity Tested	Quantity Failed	% Yield
Hermetic Controls	172	2	98.8
Standard SOIC	173	10	94.2
ChipSeal SOIC	320	4	98.8
NoFOx SOIC	278	4	98.6
Standard DIP	104	4	96.2
ChipSeal DIP	275	8	97.1
NoFOx DIP	269	1	99.6

6.2 *Test Design*

A variety of military and commercial standards were considered for assessing the reliability of the microcircuits with and without ChipSeal protection. Additional inputs were gathered from the Technical Advisory Panel, made up of Sematech member companies, potential industry customers, and Air Force Research Laboratory members. It was agreed that conventional device screening and qualification tests would provide a good baseline from which comparisons could be made against Sarnoff's existing database as well as to provide some insight into similar commercial data. In addition, a separate set of severe reliability tests was compiled to simulate harsh military/industrial conditions. The MIL-STD-883 and various JEDEC standards were used in this comparative reliability assessment. The test plan is shown schematically in Figure 19.

Moisture sensitivity tests were conducted in accordance with joint electronics standards division (JESD) A112 to determine the appropriate preconditioning conditions. Although most of the samples only qualified at Level 3 (30 °C, 60 percent RH, 192 hours) because of delaminations at the molding compound (MC)/lead frame or MC/paddle interfaces, all of the devices were preconditioned at the more severe Level 1 (85 °C, 85 percent RH, 168 hours) exposure. The preconditioning is designed to simulate industry solder reflow operations used during board assembly. The packages are subjected to temperature cycles to simulate shipping (5 cycles at -40/+60 °C), a pre-bake for drying (24 hr at 125 °C), moisture exposure at conditions based on the designated sensitivity level to simulate storage, solder reflow cycles (3 cycles at 220 °C) to simulate component assembly to PCBs including, water soluble flux immersion, a water rinse with ambient drying, and a final visual inspection and electrical testing.

The results of the electrical screening (MIL-STD-883, Method 5004) and qualification testing (MIL-STD-883, Method 5005) are summarized in Tables 23 and 24 for the GEM 8205 and 2505 device types respectively. Out of more than 3000 tests for each device type, less than 1 percent failures occurred, with no clear process/package incompatibilities evident.

Table 23. MIL-STD-833 Screening and Qualification Results for GEM 8205 Device Types

Package Configuration	**16 Pin DIP**						**16 Pin SOIC**					
Coating Structure	ChipSeal		NoFox		Standard		ChipSeal		NoFox		Standard	
	Quantity		Quantity		Quantity		Quantity		Quantity		Quantity	
	Pass	Fail	Pass	Fail	Pass	Fail	Pass	Fail	Pass	Fail	Pass	Fail
Test Sequence												
Init. Elec.	151	1	152	2	70	0	150	0	152	2	71	1
3-Temp. Elec.	150	0	150	0	70	0	149	1	150	0	70	0
B.I. 168 hr	150	0	150	0	70	0	149	0			70	0
Post B.I. Elec.			150	0	70	0					68	2
Bond Strength	4	0	3	1	4	0	4	0	4	0	4	0
1000 Hr. Life	45	0	45	0	45	0	45	0	45	0	45	0
End point Elec.	44	1	45	0	45	0			45	0		
Thermal Shock	15	0	15	0	15	0	15	0	15	0	15	0
Temp. Cycle	15	0	15	0	15	0	15	0	15	0	15	0
Moisture Resistance	15	0	15	0	15	0	15	0	15	0	15	0
End Point Elec.	14	1	14	1	15	0	15	0	15	0	15	0
Final Electrical			59	1	60	0						

Table 24. MIL-STD-833 Screening and Qualification Results for GEM 2505 Device Types

Package Configuration	**24 Pin DIP**						**24 Pin SOIC**					
Coating Structure	ChipSeal		NoFox		Standard		ChipSeal		NoFox		Standard	
	Quantity		Quantity		Quantity		Quantity		Quantity		Quantity	
	Pass	Fail	Pass	Fail	Pass	Fail	Pass	Fail	Pass	Fail	Pass	Fail
Test Sequence												
Init. Elec.	154	4	150	0	72	2	151	1	153	3	74	4
3-Temp. Elec.	146	4	150	0	70	0	148	2	149	1	70	0
B.I. 168 hr	146	0	150	0	70	0	148	0	149	0	70	0
Post B.I. Elec.	144	2	150	0	70	0	148	0	149	0	70	0
Bond Strength	4	0	4	0	4	0	4	0	4	0	4	0
1000 Hr. Life	45	0	45	0	45	0	45	0	45	0	45	0
End point Elec.	45	0	44	1	45	0						
Thermal Shock	15	0	15	0	15	0	15	0	15	0	15	0
Temp. Cycle	15	0	15	0	15	0	15	0	15	0	15	0
Moisture Resistance	15	0	15	0	15	0	15	0	15	0	15	0
End Point Elec.	14	1	14	1	15	0	15	0	15	0	15	0
Final Electrical	56	1	58	0	60	0						

Following the preconditioning, the device groups were subdivided for the following tests. One group (50 pieces of each device type and package style) was placed in the HAST at 140 °C, and 85 percent RH with a +5 V bias or ground on alternating input pins and the outputs left open or grounded through a 2.5 K resistor to minimize current draw. The second group (23 pieces of each type and style) was exposed to 2000 temperature cycles (-65 to +150 °C) followed by salt fog exposure (0.5 percent) at 35 °C.

6.3 *Reliability Test Results*

After preconditioning, the devices designated for HAST and temperature cycle/salt fog testing were again tested to determine the impact of the preconditioning on yield. The data is summarized in Table 25. Again, the results indicate that the ChipSeal process is compatible and did not reduce the device packaging yields. It should be noted that a number of 8205 standard SOIC devices did fail the preconditioning exposure.

The temperature cycle tests, Table 26, did not result in enough failures to differentiate the device treatments or package styles in terms of reliability. After 24 hours of salt fog exposure, the hermetic packaged devices and the plastic SOIC devices still showed equivalent reliability. Although the salt fog did not affect the encapsulated devices, it did produce significant failures for the bare die in the D-packages. Approximately 90 percent of the standard devices failed compared to approximately 15 percent of the ChipSeal processed devices. The NoFOx configuration did not perform as well as the ChipSeal devices. Failure analyses, performed by Oneida Research, were not conclusive but indicate possible corrosion of the underlying metal due to incomplete coverage or sealing at the bondpad windows.

Table 25. Postconditioning Device Yields (JESD22-A113, Level 1)(85 °C, 85% RH, 168 hrs)

GEM 8205, High Speed Binary Decoder			
Test Configuration	Quantity Tested	Quantity Failed	% Yield
Hermetic Controls	92	0	100.0
Standard SOIC	92	23	75.0
ChipSeal SOIC	80	6	92.5
NoFOx SOIC	92	2	97.8
Standard DIP	100	3	97.0
ChipSeal DIP	106	0	100.0
NoFOx DIP	105	0	100.0

Gem 2505, Complement Multiplier			
Test Configuration	Quantity Tested	Quantity Failed	% Yield
Hermetic Controls	89	3	96.6
Standard SOIC	79	0	100.0
ChipSeal SOIC	89	0	100.0
NoFOx SOIC	108	4	96.3
Standard DIP	98	4	95.9
ChipSeal DIP	113	2	98.2
NoFOx DIP	108	1	99.1

Table 26. Electrical Test Results for Temperature Cycle and Salt Fog Exposures

GEM 8205, High Speed Binary Decoder							
Test Configuration	Quantity	Cumulative Results (% Failure)					
		100 c	500 c	1000 c	1500 c	1000 c	Salt Fog
Hermetic Controls	23	0	0	0	0	0	0
Standard SOIC	23	0	0	0	0	0	0
Standard DIP	23	0	0	0	0	0	96
ChipSeal SOIC	23	4	4	4	4	4	4
ChipSeal DIP	23	0	0	0	0	0	9
NoFOx SOIC	23	0	0	0	0	0	0
NoFOx DIP	23	0	4	4	4	4	96

GEM 2505, Complement Multiplier							
Test Configuration	Quantity	Cumulative Results (% Failure)					
		100 c	500 c	1000 c	1500 c	1000 c	Salt Fog
Hermetic Controls	23	0	0	0	0	0	0
Standard SOIC	23	9	9	9	9	9	9
Standard DIP	23	0	0	0	4	4	83
ChipSeal SOIC	23	0	0	0	0	0	0
ChipSeal DIP	23	0	0	0	4	4	22
NoFOx SOIC	23	0	0	0	0	0	0
NoFOx DIP	23	0	0	0	0	0	96

c = # of cycles

The cumulative failures through 1000 hours of HAST environmental stress testing are summarized in Tables 27 and 28 for each of the device types. Since the results indicate that there was little difference in the performance of the two integrated circuit designs, the results are combined in Figures 20 and 21 for the SOIC and DIP package configurations.

The first performance differentiation is evident for the SOIC encapsulated devices at 350 hours and at 150 hours for the bare die (D-package) configurations. At 350 hours, all the standard bare die (standard D-package) samples for both device types had failed. All functional failures were due to single or multiple open circuits caused by bondpad corrosion.

For the standard SOICs, parametric shifts, which were first observed at 100 hours, became significant by 500 hours and became functional failures in subsequent test increments. Also, at 500 hours some discrimination is evident for the encapsulated NoFOx samples (NoFOx SOIC) as well as the bare NoFOx samples (NoFOx DIP).

At 1000 hours, nearly all of the standard SOIC samples had failed (99 percent) compared to an average 8 percent for the encapsulated ChipSeal samples. For the bare die configurations, the number of ChipSeal failures is even more comparable to that of the Hermetic controls (4 percent versus 2 percent) indicating that the ChipSeal inorganic coatings can provide near hermetic reliability. Also, the combined reliability of both the ChipSeal coated plastic encapsulated devices and the open cavity devices are equivalent (8 percent versus 4 percent failures), indicating that the plastic overmolding is providing little if any additional protection.

Table 27. Cumulative HAST Failures for Hermetic Controls and Plastic Encapsulated SOIC Configurations

GEM 8205, High Speed Binary Decoder							
Test Configuration	Quantity	Cumulative Results (% Failure)					
		50 Hrs	150 Hrs	350 Hrs	500 Hrs	750 Hrs	1000 Hrs
Hermetic Controls	25	0	0	0	0	4	4
Standard SOIC	50	0	0	10	14(34)	22(94)	28(98)
ChipSeal SOIC	50	0	0	2	2	2(4)	6(10)
NoFOx SOIC	50	2	2	4	8	10(38)	10(16)

GEM 2505, Complement Multiplier							
Test Configuration	Quantity	Cumulative Results (% Failure)					
		50 Hrs	150 Hrs	350 Hrs	500 Hrs	750 Hrs	1000 Hrs
Hermetic Controls	25	0	0	0	4	4	4
Standard SOIC	50	0	0	4	48(60)	62(100)	STOP
ChipSeal SOIC	50	0	0	2	4	4(12)	4
NoFOx SOIC	50	0	0	2	4	4	4(10)

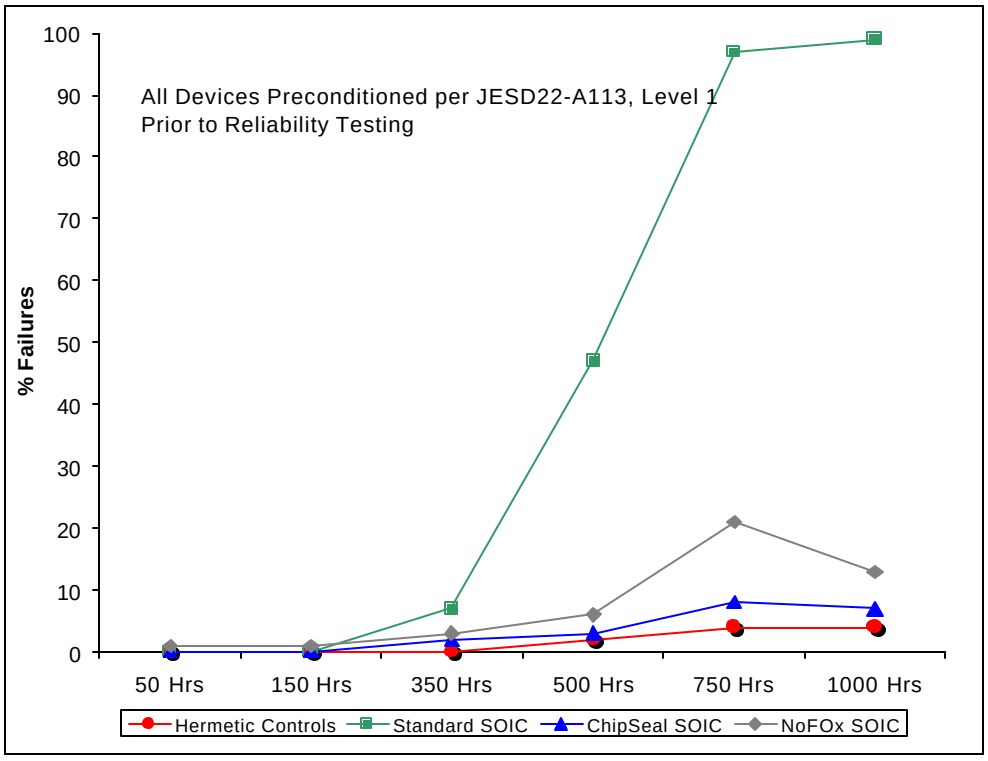
(#) indicates device results from both functional and parametric failures

Table 28. Cumulative HAST Failures for Hermetic Controls and Open Cavity (Bare Die) Configurations

GEM 8205, High Speed Binary Decoder							
Test Configuration	Quantity	Cumulative Results (% Failure)					
		50 Hrs	150 Hrs	350 Hrs	500 Hrs	750 Hrs	1000 Hrs
Hermetic Controls	25	0	0	0	0	0	0
Standard DIP	50	0	10	100	100	100	100
ChipSeal DIP	50	0	0	2	2	4	4
NoFOx DIP	50	0	0	12	30	62	82

GEM 2505, Complement Multiplier							
Test Configuration	Quantity	Cumulative Results (% Failure)					
		50 Hrs	150 Hrs	350 Hrs	500 Hrs	750 Hrs	1000 Hrs
Hermetic Controls	25	0	(4)	4	4	4	4
Standard DIP	50	4	4	100	100	100	100
ChipSeal DIP	50	0	0	0	2	4	4
NoFOx DIP	50	0	0	4	10	324	46

(#) indicates device results from both functional and parametric failures



BiCMOS Gate Arrays: GEM 8205 & 2505 Devices
Functional and Parametric Failures

Figure 20. Performance of Plastic SOICs in 140 °C HAST

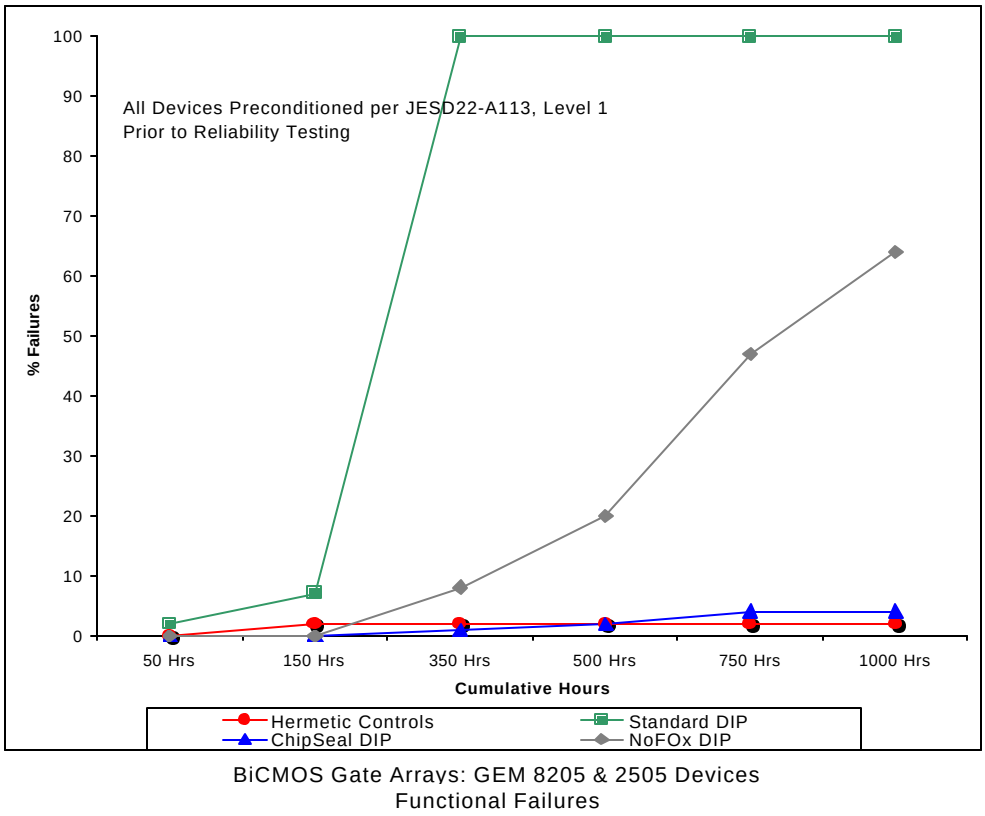


Figure 21. Performance of Bare Die in 140 °C HAST

Failure analyses was conducted on one failed ChipSeal open cavity device and several plastic encapsulated devices of the Standard, ChipSeal, and NoFOx configurations by Oneida Research:

- None of the failures were attributed to the dielectric passivation. The weak link was consistently the interconnect region.
- The overlap of the high reliability metal bondpad onto the passivation showed peeling in many cases for both the ChipSeal and NoFOx configurations. Some peeling was also evident on new die. This is the region in which an undercut of the metal during bondpad etch could be a problem. However, the failures for the particular devices examined could not be directly linked to the observation.
- For the plastic SOICs, wire bond pull strength tests on all device configurations consistently showed weak connections. In isolated instances, penetration of the bondpad surface from the wire bonding process was observed. Also, in one instance, the entire gold layer separated from the device with the bond wire during the pull test.
- For the open cavity device, nickel was found on the die bondpads. It appeared to have diffused through the gold out onto the device surface. The source of the nickel is the metallization used in the ceramic carrier.
- For the SOIC and bare die, electro migration of Al at the input diode junction was observed.

6.4 *GEM Device Reliability Testing Conclusions*

1. The environmental stress performance of the GEM ICs processed with ChipSeal coatings (either in plastic or open cavity packages) is equal to that measured on control devices in hermetic packages.
2. The reliability of both the ChipSeal plastic encapsulated devices and the ChipSeal open cavity devices is equivalent.
3. The plastic molding compound does not provide environmental protection above that provided by the ChipSeal coatings.
4. Temperature cycling tests did not produce enough failures to discriminate between any of the configurations tested.
5. The salt fog exposure was not capable of distinguishing between ChipSeal and standard devices in plastic packages.
6. HAST testing provided the only discriminating results for encapsulated devices.
7. The NoFOx coating configuration is subject to higher failure rates in both the encapsulated and bare die packages, indicating possible incomplete TiW step coverage at the bondpad periphery. FOx solves this issue through planarization of the window opening.

7. Solder Bump Technology

The MCMs could benefit the most from the ChipSeal technology [10]. In their preferred configuration, MCMs will be assembled using flip-chip technology. Flip-chip solder bump technology requires the use of a substrate to provide the interconnect between the various devices which comprise the module. The evaluation of ChipSeal for flip-chip applications requires two tasks: 1) the design and preparation of reliable test substrates, and 2) the development of a compatible solder bumping process. The technology flow is shown in Figure 22. MCNC conducted these activities, with transfer of the plasma-SiC technology from Dow Corning and the supply of device designs and nonfunctional test devices by Sarnoff. A schematic of the flip-chip/test substrate configuration is shown in Figure 23.

7.1 *Test Substrates*

Based on bondpad layouts for the test devices, MCNC designed silicon based test substrates that would interface directly with a test socket. This involved the design and preparation of all of the masks for fabrication of the substrates (16/wafer) and solder bumping of the devices. The substrates were fabricated with a plasma-SiC coating to provide environmental reliability equivalent to that of the test die. The final process established at MCNC provided a 750 Å/min deposition rate with minimal particulate generation and sufficient uniformity for the substrate application. A CF_4/O_2 etch process was developed that provided a 58° sidewall geometry.

7.2 *Solder Bump Process*

The MCNC standard solder bump process requires a sloped sidewall for the bondpad windows. Most bondpad windows, including those on the test devices fabricated by Sarnoff for this program, have vertical walls. An MCNC process converts the window profile to a new orientation that involves the application and patterning of a thick intermediate dielectric layer, which requires a 400 °C cure. Concerns that this high process temperature would be detrimental to the devices which had not seen temperatures > 350 °C during their previous processing lead to the decision that no special windows would be fabricated unless absolutely necessary. Sample device wafers with standard bondpad openings were supplied for initial tests of the bump process compatibility and bump metal adhesion to the silicon carbide.

The standard UBM process, which consisted of a proprietary Cr/CrCu/Cu/Au metallization system, was applied to the above wafers [11]. The adhesion to the plasma-SiC was sufficient to allow successful bumping of some of the blank wafers. The blanket UBM layers, deposited on simulated device wafers, demonstrated that 50 percent coverage of the existing bondpad sidewall topography could be achieved with the standard UBM process (i.e., the sidewall, which is normal to the wafer surface, has a deposition rate which is approximately 50 percent to that of the planar surface). Thus, there was no need to re-optimize the UBM process. Both the ChipSeal passivation and the standard device window geometry are compatible with the standard bumping process.

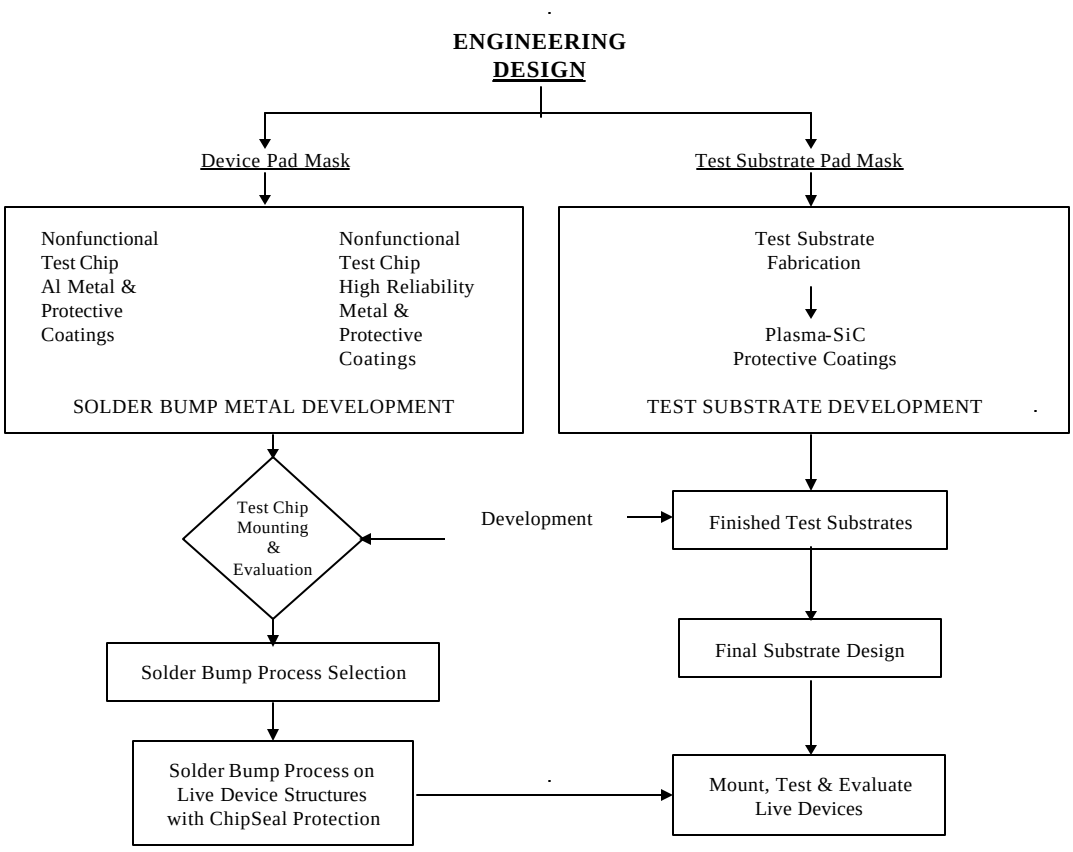


Figure 22. Solder Bump Technology Flow/Pad Mask Design

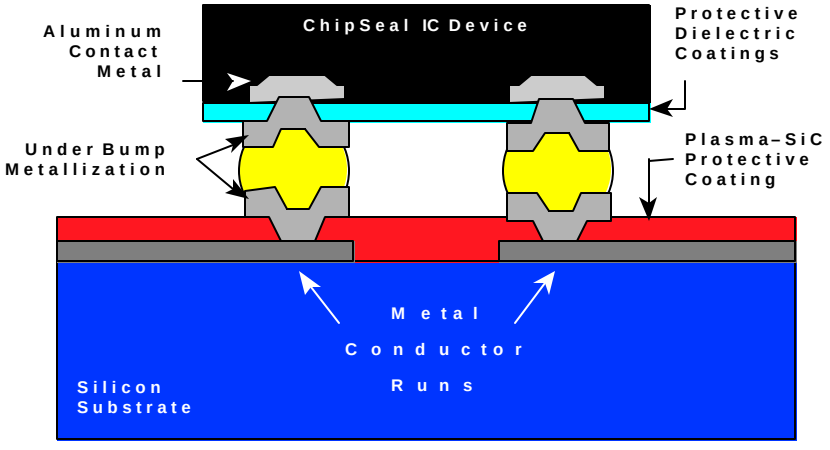


Figure 23. Schematic Cross-Section of a Solder Bumped ChipSeal Processed IC and Test Substrate for Flip-Chip Reliability Evaluations

For the first set of nonfunctional test samples, the bump metallization processes appeared to proceed normally. The UBM deposition, solder electroplating, and the UBM etch were all performed without incident. However, after solder reflow, a significant number of bumps exhibited internal voids (Figure 24). A second reflow eliminated the voids open to the surface (Figure 25), but some internal voids still existed. Removal of the solder and examination of the bond area indicated that there may have been discontinuities in the UBM step coverage (Figure 26). A re-examination of the original bondpad surfaces indicated a higher than normal metal roughness that could have contributed to thin or incomplete coverage of the UBM.

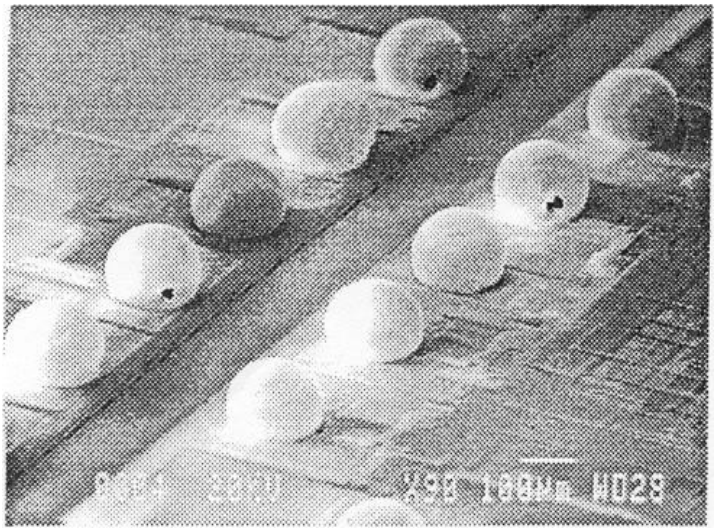


Figure 24. Photomicrograph of Bumps after Initial Reflow

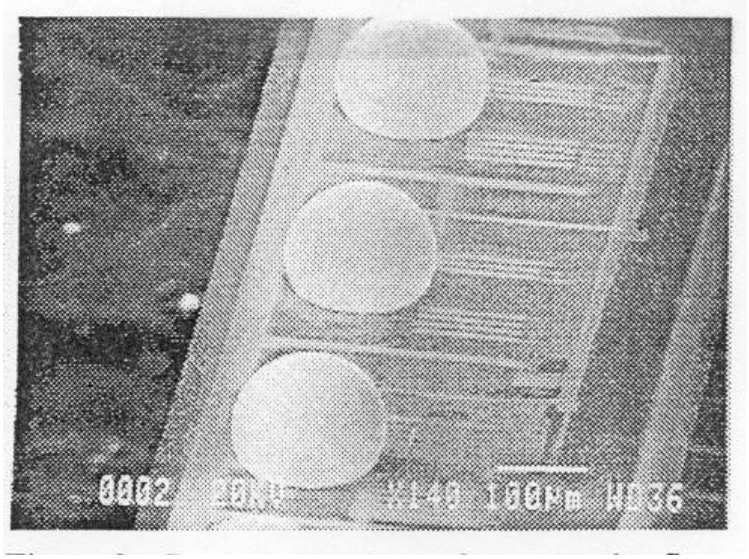


Figure 25. Bump Appearance after Second Reflow

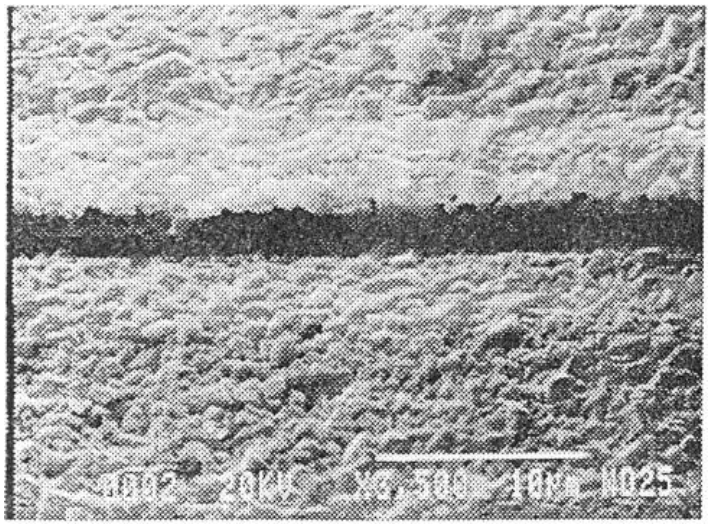


Figure 26. SEM of Bond Area Sidewall where UBM Formation is Incomplete

A second set of mechanical samples was put through the same bump process but with an increased deposition thickness (0.5 µm) for the UBM. None of the bumps exhibited voids after reflow. It is believed that the increased UBM thickness produced better step coverage, allowing proper bump formation. These bumps also exhibited improved mechanical integrity. The improved step coverage was subsequently verified by microscopic examination.

To further assess the mechanical integrity of the solder bumps, flip-chip test assemblies were put through temperature cycling tests. The test samples were exposed to -40 °C then 125 °C with cycle times of 6 minutes for a total of 500 cycles. Analysis of the test structures showed that temperature cycling produced no change in the Kelvin resistance of the bump/UBM interface or any degradation of the tensile strength of the bumps. The shear strength of the solder bumped assemblies after temperature cycling was measured. The results were significantly higher than that measured on previously temp cycled samples. In addition, tests on the nonfunctional die assemblies also showed no effect on the mechanical integrity of the bumps after thermal cycling. From these results it was concluded that the solder bump process and bump integrity were sufficient to proceed with flip-chip fabrication and testing on ChipSeal functional die. These results show that the ChipSeal process and materials are compatible with flip-chip processes and demonstrates that the two can be integrated for MCM applications.

7.3 *Mounting and Reliability Testing – Flip-Chip Configurations*

7.3.1 Flip-Chip Assembly

The assembly and testing of the solder bumped devices were conducted separately from that of the wire bond devices. A set of three fully functional device wafers and seven mechanical test wafers were reserved for the solder bump evaluations. These wafers did not have the high reliability metallization applied to the bondpads. To facilitate testing in the flip-chip mount

configuration, silicon substrates were designed and fabricated with Ti/Al(Cu)Ti metallized traces to interconnect between the die and substrate test socket. The substrate surfaces were protected with plasma-SiC similar to that used in the ChipSeal process. The substrate and die contacts were coated with MCNC's proprietary Cr/CrCu/Cu/Au metallization to form solder-wettable surfaces for reliable flip-chip bonding. Photographs of the bumped functional die are shown in Figure 27 and a cross-section of a bump contact region is shown in Figure 28. One hundred die were assembled for reliability testing. Approximately one half of the assemblies were underfilled with an epoxy. This test configuration was included to provide an evaluation of the compatibility of the plasma-SiC on the die and substrate with a typical underfill assembly. Since the test substrates were made of silicon, the issues regarding a mismatch of the coefficient of thermal expansion (CTE) between the die and substrate are not a concern.

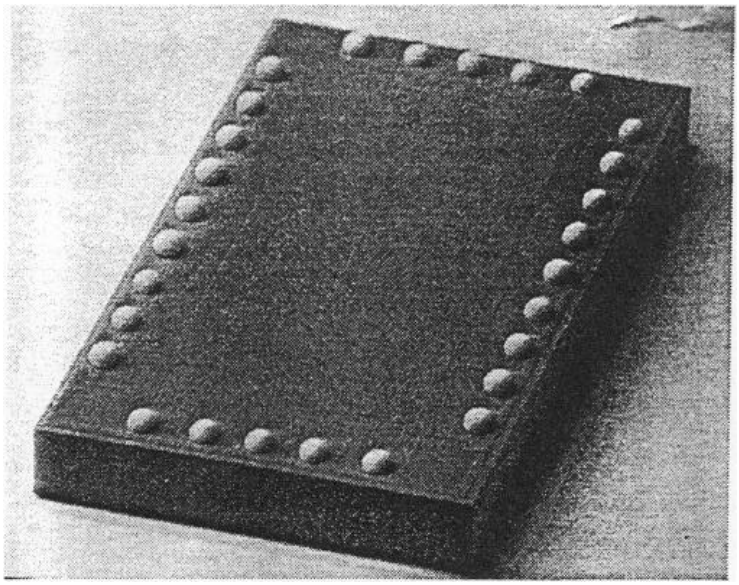


Figure 27. Solder Bumped, Functional GEM Die

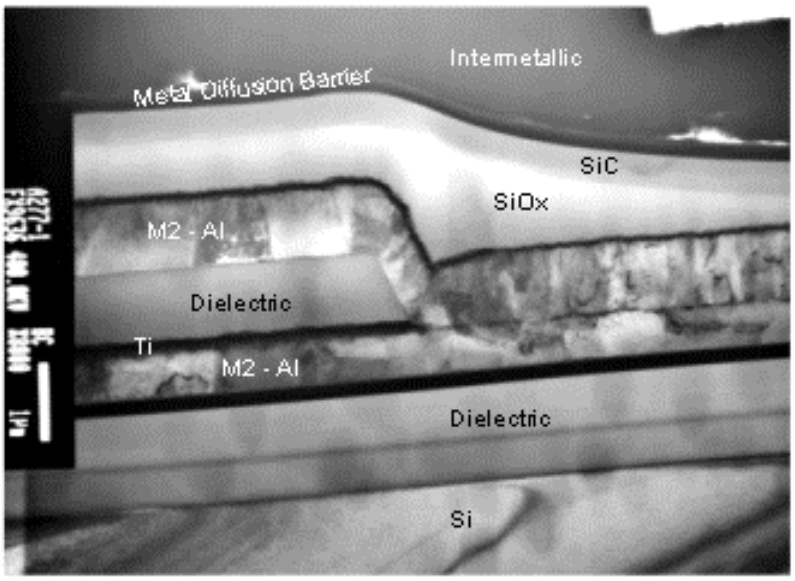


Figure 28. TEM Cross-Section of a ChipSeal Processed, Solder Bump Device
(The smoothing of the window edge by the spin-on oxide can be seen at the center of the figure)

7.3.2 Test Design

The flip-chip test flow is shown in Figure 29. Following initial electrical tests, the reliability of the assemblies was tested using a burn-in test (168 hours at 150 °C), temperature cycling (500 cycles, -65 to +125 °C), and a salt fog exposure (24 hours).

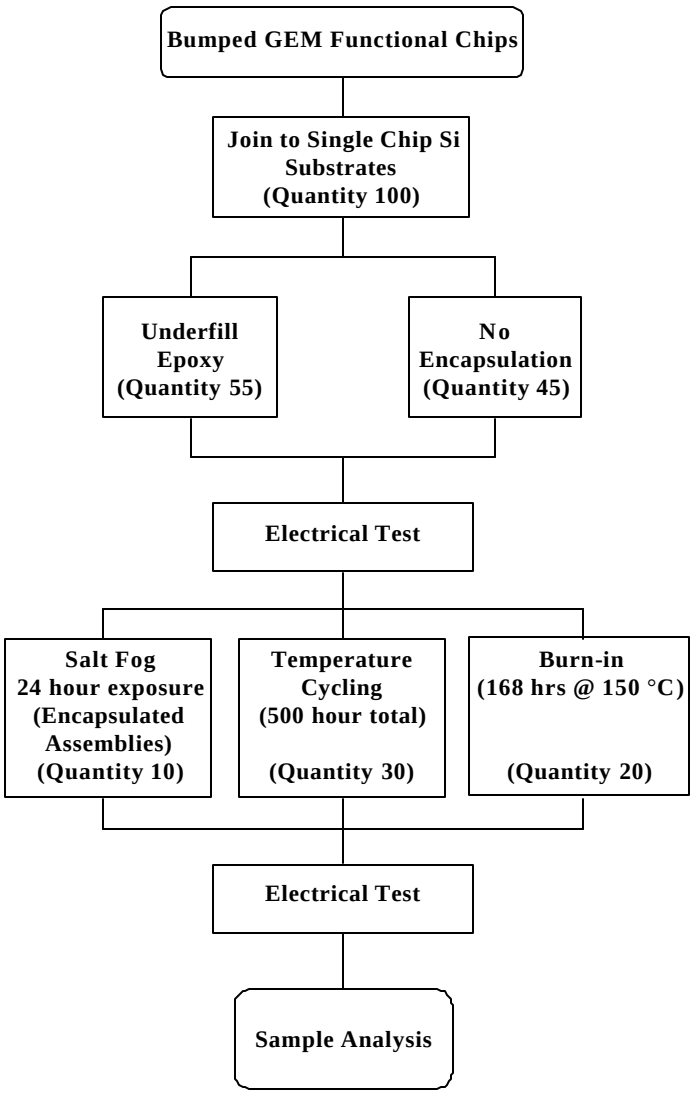


Figure 29. Bumped Die Reliability Test Plan

7.3.3 Test Results

The initial electrical tests showed that 54 of the 100 device assemblies were fully functional and an additional 22 assemblies passed continuity tests. For the remainder, the substrates were either damaged or broken from insertion or removal from the test sockets. Problems were also encountered during post-stress parametric testing. In nearly all cases, the substrate interconnections, solder bumps, and I/O circuitry remained intact, but logic errors internal to the devices were detected. Because of the test complications imposed by the mounting and test setup, only qualitative information on reliability could be obtained. The burn-in tests typically did not result in a decrease in bump electrical continuity or mechanical strength. Both the temperature cycling and salt fog exposures resulted in a significant decrease in mechanical strength and integrity of the bumps. In all cases, the underfill encapsulated devices outperformed the others.

The failures that were observed were associated with the choice of materials for the substrate and the method of testing. The environmental testing (temperature cycling and salt fog) confirmed the intrinsic vulnerability of solder bumps to mechanical stress and corrosive environments. The underfill provided the additional strength and protection of the solder as it is intended to do.

If the ChipSeal process is used with solder bumped devices, a few issues need to be addressed:

1. The SiO_x layer was undercut during the etch of the UBM. This occurred at the edge of the die where the SiO_x was exposed when the ChipSeal dielectrics were etched to open the bondpads and streets. This can be avoided by redesign of the etch masks to avoid opening the streets. The streets were used to align the masks to the wafers in lieu of adding alignment keys or sacrificing die.
2. The design and materials of construction of the substrate needs to be mechanically compatible and as environmentally reliable as the chip.
3. A method for protection of the solder needs to be incorporated for long term reliability.

8. Phase II - ChipSeal Implementation

The tasks completed in Phase I established the process fundamentals and demonstrated the hermetic reliability performance of the ChipSeal process utilizing the Sarnoff BiCMOS GEM devices. The objective of Phase II is to scale the process technology to accommodate 150 mm diameter wafers and demonstrate the applicability and process compatibility to a variety of commercial and proprietary device types.

The activities include the following:

- Scale and optimize the high-reliability metallization processes
- Scale and optimize the dielectric coating application processes
- Demonstrate process compatibility on a significant number of commercial and proprietary device types.

8.1 *Application of ChipSeal to Multiple Device Types*

Encouraged by the reliability results on the GEM devices in Phase I, Dow Corning in collaboration with Rockwell Collins also embarked on a joint investigation of the protection provided by ChipSeal processed devices in functional MCMs. The commercial device types chosen for the process compatibility evaluation were based on two module designs provided by Rockwell. The first was a data processing module incorporating multiple analog ICs (eight differential amplifiers and two quad Opamps). The other was a digital GPS based navigational module using four digital ICs (a high speed microprocessor, a digital signal processor, two flash memory chips and two RAM memories). Both modules had a combination of standard plastic encapsulated microcircuits (PEMs), which required surface mount assembly, and bare die. The experimental design called for the assembly and testing of demonstration modules using both wire bond (chip-up) and solder bumped (flip-chip) interconnect configurations on laminate substrates. The design, assembly, and testing of the modules was funded jointly by Dow Corning and Rockwell.

8.2 *Establish Live Device Wafer Processing Capability for 150 mm Wafers*

8.2.1 Dielectric Film Deposition

8.2.1.1 ***FOx Coating***

A 150 mm wafer conversion kit was purchased for the SEMIX spin coating unit. The same coating parameters were used for 150 mm wafers as for 100 mm wafers, with the exception of a proportional increase in dispense volume and the hotplate bake time (the final process parameters are shown in Volume 2). After adjustments were completed, typical coating thickness and uniformity were 3500 ± 30 Å (Process specification is 3500 ± 200 Å.) [4].

The intensity of the SiH peak at 2260 cm^{-1} in the IR spectra is used to assess the completeness of the cure. A final cure temperature of 400 °C for 20 minutes was selected based on an approximate 65 percent reduction in peak height. The final cure of the FOx films on 100 mm wafers is normally conducted in a dedicated nitrogen-purged tube furnace. Since the existing

furnace could not accommodate 150 mm wafers, a process was developed which would allow the final cure to be conducted insitu in the ASM PECVD tube furnace. The system is preheated to 400 °C. After insertion of the wafers, the control temperature was reset and the furnace allowed to cool slowly to the prescribed 350 °C PECVD deposition temperature. Results on 150 mm test wafers indicated no apparent differences in resulting SiO_x film properties and the combined SiC/SiO_x etch characteristics, compared to the previous procedures used for 100 mm wafers.

8.2.1.2 ***SiC Deposition***

The ASM PECVD system at Sarnoff required physical modification to accommodate 150 mm wafers. This involved the fabrication of larger diameter graphite electrodes and procurement of a 150 mm wafer carrier. Initial test depositions conducted with the new electrodes and carrier at the same parameters used for the 100 mm wafers were unsatisfactory. Higher power settings were required to increase deposition rate and lower gas pressure to reduce arcing. Because of the increased wafer area and reduced power density, the deposition rate is significantly lower for the 150mm wafers than for the 100 mm wafers. Typical rates are 240 and 550 Å/min respectively [4].

Another application that provided an interesting contrast to the standard processes developed within this program, and included here for completeness, is silicon-on-sapphire (SOS). The SiC deposition parameters on SOS are very different than on silicon. Initial tests using the parameters for 100 mm silicon wafers showed a two fold reduction in deposition rate and poor uniformity when the SOS wafers were placed face-to-face in the PECVD furnace. After several trials, conditions were established that provided a nominal 540 Å/min deposition rate with all the wafers arranged facing a bare graphite electrode. A comparison of SiC deposition rates is shown in Table 29.

Table 29. Silicon Carbide Deposition Parameters

Diameter, mm	**Pressure, Torr**	**Power, W**	**3MS Flow, sccm**	**Ar Flow, sccm**
Silicon Wafers				
150	1	200	500	1000
100	2	200	500	1000
SOS Wafers				
100	2	300	500	500

Using these parameters, the thickness uniformity across the wafers and between wafer positions within the furnace tube is better than ±7 percent.

8.3 *Wafer Patterning*

8.3.1 Aligner Procurement

To pattern the 150 mm wafers a Quintel Q-7000 mask aligner was procured. The unit has both contact and proximity exposure modes, programmable 3-point proximity calibration, a motorized

x, y, and theta micrometer stage, a 7 by 7 inch mask holder, split field optical alignment, manual load 150 mm wafer chucks, and a 350 W mercury (Hg) exposure lamp.

A proximity gap of 30 µm was selected for use for the ChipSeal 150 mm wafers. Initial qualifications were conducted with both clear-field and dark-field masks. Double images resulting from the lack of an anti-reflection coating on the collimating lens was corrected by removal of the lens. For 150 mm wafers, this resulted in a 4 µm runout from center to edge for the bondpad opening location. This did not present an immediate problem for the program wafers because of the negative16 µm bias design rules chosen to pattern the bondpads. A new anti-reflective collimating lens was ordered to correct the problem.

8.3.2 Photoresist Processing

Phase II of the ChipSeal program required establishing, at Sarnoff, a 150 mm photoresist patterning and stripping capability. Previous facilities used to pattern large area display plates that were modified to handle 150 mm wafers by the procurement of vacuum chucks for the resist spinner and developer and quartz ware for the plasma etcher and bake ovens.

After SiC deposition or high-rel metal depositions, the wafers are coated with photoresist. A positive photoresist material is spun onto the wafers using an automatic dynamic dispense system at 750 rpm. The dispense arm oscillates from the center to just inside the edge of the wafer. Nominal resist volume is 10 ml. The wafers are soft baked in a batch air convection oven for 30 minutes at 100 °C.

The final resist thickness is 2.8 µm. A thick resist coating is used for the SiC etch because the etch process erodes the resist at the same rate as the SiC. High points on the wafer surface need to be covered sufficiently to prevent etching of the dielectric. A thick resist coating is not needed for the high-rel metal wet etch, but the same coating thickness is typically used to promote process standardization.

The resist film is exposed on the Quintel proximity printer at a nominal 300 mJ/cm^2. A metal-free developer at a 47 percent concentration is used to develop the pattern. A develop time of 3 minutes was used in the large substrate spin developer or in the batch mode. The batch mode was used for all 150 mm wafer lots processed in the program. After development, the resist is baked at 140 °C for 60 minutes in a batch convection oven.

Numerous 150mm wafers were exposed and developed with ChipSeal bondpad and reverse bondpad masks. The wall profile of the resist was characterized. A sloped profile is needed to produce an appropriately sloped etch profile for the SiO_x/SiC bondpad opening. The Quintel Q-7000 aligner and the new photo process readily produced acceptable resist profiles. A typical profile, shown in Figure 30, has a wall angle at the bottom of 50 degrees or less with respect to horizontal.

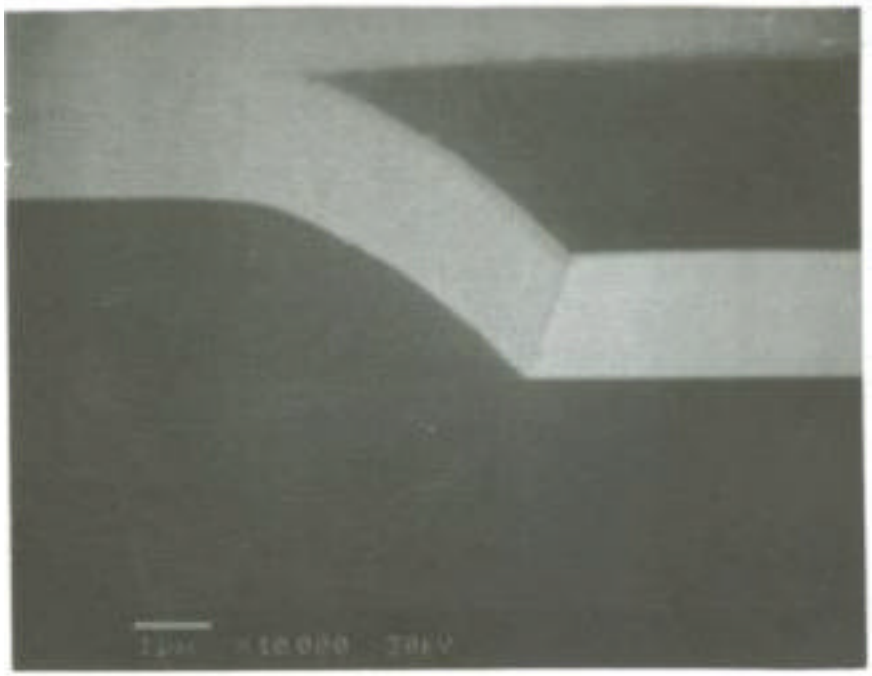


Figure 30. SEM Cross-Section of Resist Profile from Proximity Aligner

After the SiC or high-rel metal etch, the photoresist is stripped in a Branson barrel stripper in O_2 plasma. The thickness of the resist and the large size of the wafers make it necessary to use two 90 minute strip cycles. Leaving at least three extra empty slots between wafers in the quartz boat will enhance the stripping process. After dry stripping, the wafers are dump rinsed and IPA vapor dried to remove any water soluble residues on the wafer surfaces.

8.3.3 SiO_x/SiC Etch

Phase II of the program required establishing 150 mm dry etch capability at Sarnoff. Etch rate data for the SiO_x/SiC coatings were collected for various process conditions in the ANELVA reactive ion etcher. Acceptable etch rates and wall profile results can be obtained under a variety of conditions. The process also exhibits significant loading effects.

The etch profile for the SiO_x/SiC films is shown in SEM cross-sections in Figure 31. The taper on the SiO_x film is 45°, and on the SiC film, even shallower -30°. These profiles are consistent with the relative measured etch rates for the resist/SiO_x/SiC film stack. All profiles are less than 55° with respect to horizontal. The etch conditions chosen for processing device lots are as follows: Pressure = 150 Torr; Power = 500 W; and CF_4 flow rate = 60 sccm.

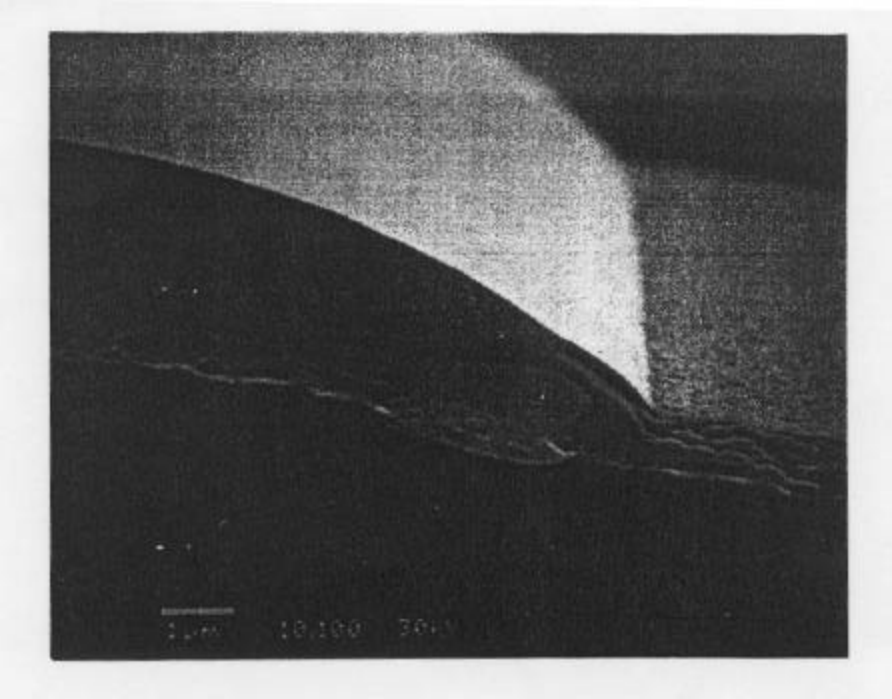


Figure 31. SEM Cross-Section of SiC and SiO_x Films After Etch

A number of different aspects of the etch process were investigated in the ANELVA reactive ion etcher during Phase II. These included the addition of O_2 to the etch gas; loading effects of the resist, SiC, and SiO_x etch rates; and the independent determination of the resist etch on the presence of SiC and SiO_x. Figures 32-34 display the etch rate data collected for these studies. The etch rates were determined using a Rudolph thin film monitor. Refractive index settings on 1.40, 1.64, and 2.45 were used for the SiO_x, resist and SiC films, respectively. Special substrates with blanket depositions of either a SiO_x or SiC coating were used with nine 7 by 7 mm openings in the patterned resist film. Etch rates were determined in at least five of these locations on every wafer. The average etch rate is reported. The SiO_x and SiC etch rates were determined in independent experiments. The SiO_x and SiC etch uniformity across the wafer for all conditions studied was ± 5 percent. The centers of the wafers appear to etch somewhat slower than the outer edges. The etch rate uniformity for the resist was better than that observed for the dielectric films, ± 3 percent.

Figure 32 shows the etch rate data for the SiC and resist as a function of the number of wafers in the etch chamber. For multiple wafer experiments, etch rates were measured on all wafers, and the average whole wafer etch rate was reported. For both etch gas compositions that are plotted in Figure 32, both the SiC and resist etch rates decrease with increased wafer loads. The resist etch rate decreases more rapidly than the SiC rate and approaches that of SiC with a four wafer load.

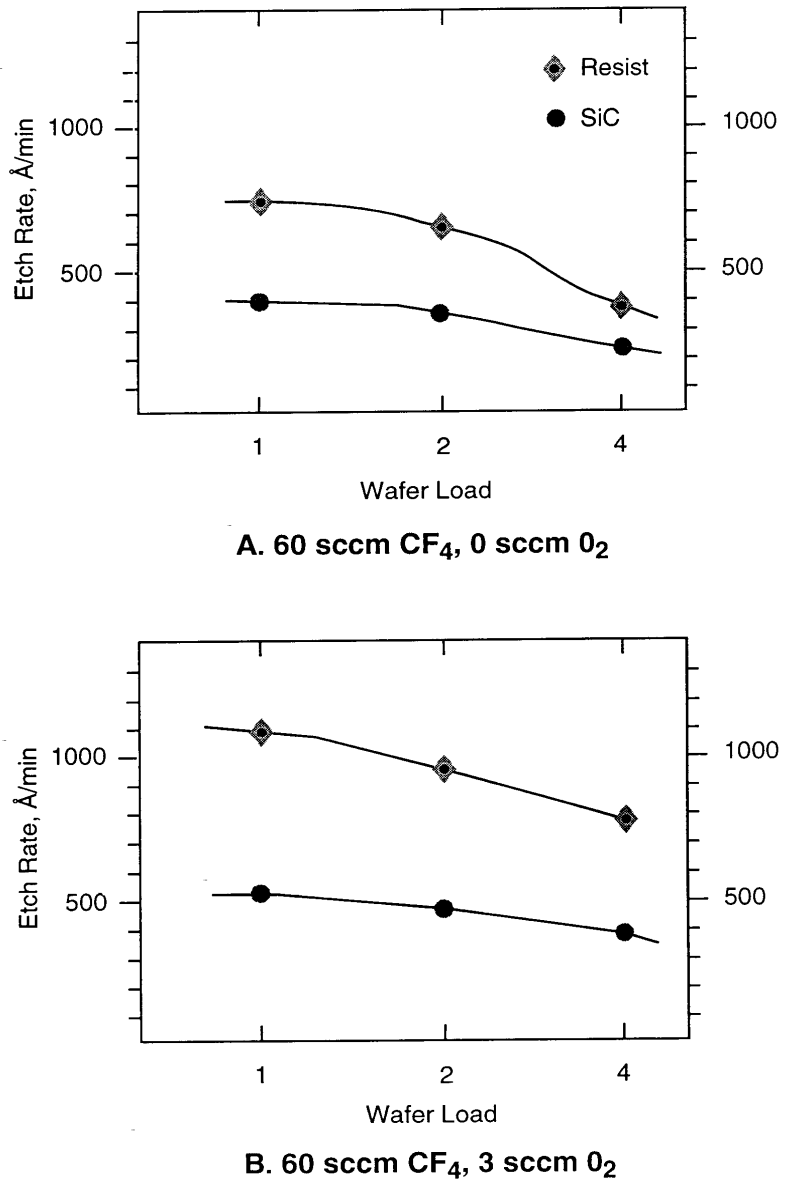


Figure 32. Etch Rates of SiC and Resist Films for Different Wafer Loads

Figure 33 shows a similar comparison of the FOx derived SiO_x and resist etch rates. The resist etch rate was measured in the presence of the SiO_x material and absence of the SiC. The resist etch rates are, to a first approximation, the same in the presence of both materials. However, for all of the measured conditions, the resist etch rate in the presence of SiO_x appears to be slightly higher (2 to 3 percent) than that in the presence of SiC. The resist rate again decreases noticeably with increasing wafer load in the presence of SiO_x. The SiO_x etch rate, however, remains relatively constant with increasing wafer loads. Only a small decrease in the SiO_x etch rate is observed. The SiO_x film etch rates are all greater than the corresponding SiC etch rates shown in Figure 32. At the high wafer load (four) the resist etch rate has dropped below that of SiO_x for the etch gas composition containing no oxygen. The resist rate for all wafer loads remains high enough to produce acceptable taper on the SiC and SiO_x profiles under all etch conditions.

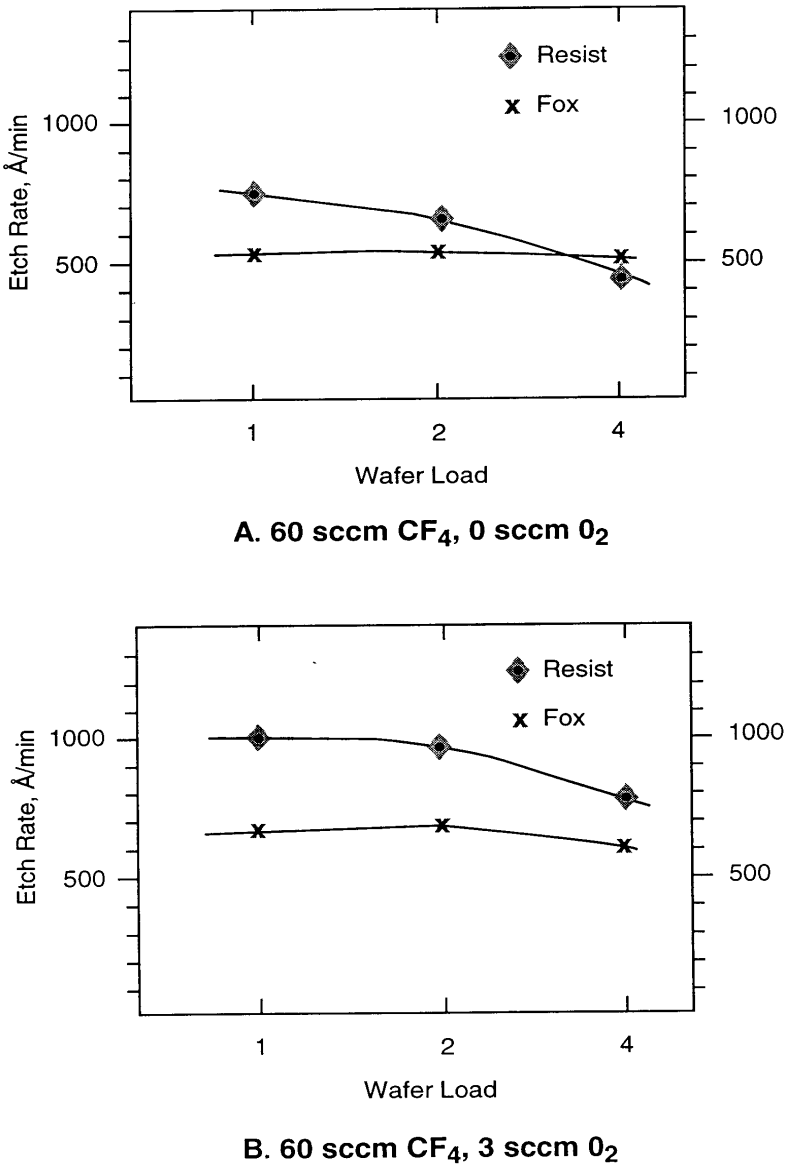


Figure 33. Etch Rates of SiO_x and Resist Films for Different Wafer Loads

Figure 34 shows the SiC and resist etch rates as a function of the amount of oxygen added to the etch gas composition. The resist etch rate increases continuously as more oxygen is added to the gas composition. The SiC etch rate increases with small additions of O_2 to the gas composition. The etch rate of the carbide has risen only 50 percent (from 400 to 600 Å/min) with the addition of the O_2. At the same gas composition that produces a 50 percent increase in the SiC etch rate, the resist etch rate has increased by more than 100 percent. Although O_2 additions can be used to enhance the SiC etch rate, it also increases the resist etch rate much more. In many cases thicker resist films would be required to etch the SiC films and avoid etching the SiC in masked (resist coated) regions of the device wafers.

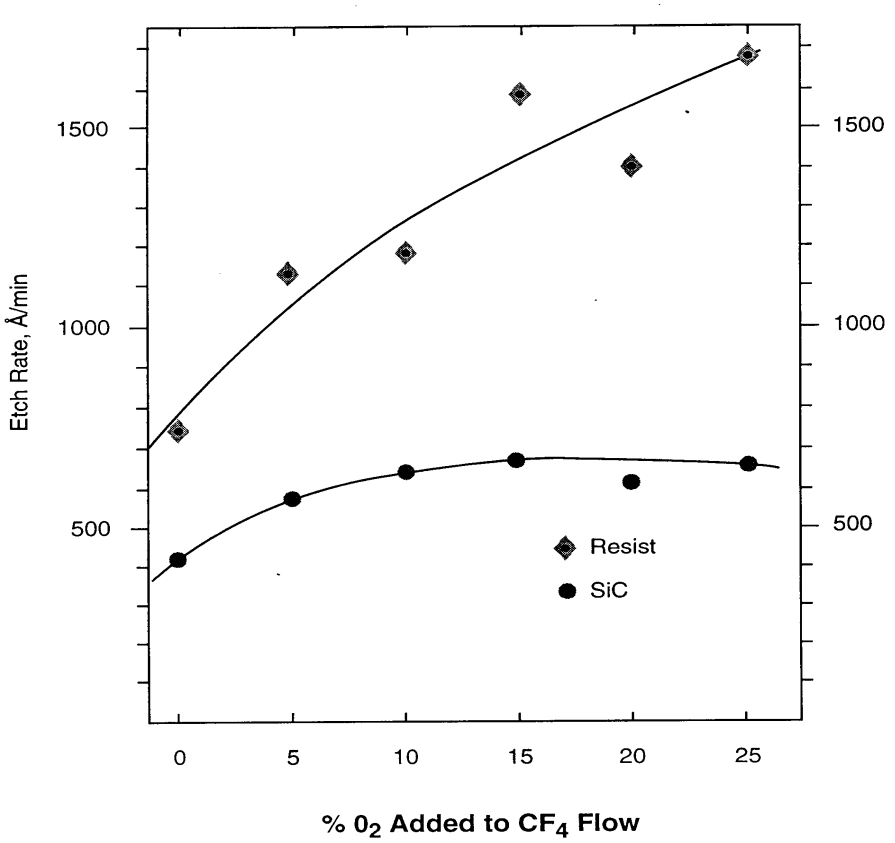


Figure 34. Etch Rates of SiC versus O_2 Content of the Etch Gas

8.4 *High-Rel Metal Deposition Process Development*

After depositing the SiO_x and SiC dielectric films and opening the bondpads, the full ChipSeal process requires the deposition and patterning of the high-rel metallization system over the Al bondpads. The high-rel metal system consists of a gold noble metal top layer and a barrier metal between the gold and the aluminum to prevent intermetallic phase formation. Phase I investigated the TiW/Au and TiN/TiW/Au metallization systems. For the latter, a thin TiW layer was added between the barrier metal and Au to assure good gold adhesion because spauling was observed in the TiN/Au samples after thermal stressing (Thermal stressing was performed in a Tencor Flexus Stress system @ 400 °C in N_2 or O_2). The TiN/TiW/Au system provided the best performance against intermetallic formation in thermal stress tests. Phase II included more studies of the high-rel metal system. The barrier metal performance as a function of thickness; the wet etching of the TiN barrier layer, and the bondpad contact resistance was investigated. The metallization deposition and wet etch process for 150 mm wafers also needed to be established. These issues are discussed in the following sections.

8.4.1 Barrier Metal Thickness Study

The Innotec V24C sputter deposition system was used to deposit various barrier metal systems with a 0.5 µm gold film overcoat on 100 mm diameter wafers. Table 30 summarizes the sheet

resistance measurements. All TiN barrier layers employed a 400 Å thick TiW layer on top to promote gold adhesion.

The sheet-rho units are milliohms-per-square. Barrier metals containing only TiW show a higher sheet-rho after FLEXUS thermal cycles. The samples with TiN barrier metals show no change in the sheet-rho after treatment. The 24-25 mΩ/sq. sheet-rho values for samples without FLEXUS treatment is typical for a sputtered gold film. These measurements agree with the optical inspection results that showed extensive degradation of the gold films with the TiW barrier layers after the FLEXUS tests. The gold films with the TiN barrier layers had no change in their appearance or their sheet-rho values.

Table 30. Flexus Test Wafers; Sheet-Rho Results

Wafer #	**Barrier Metal**	**Thickness, Å**	**Flexus**	**Sheet-Rho, mW**
13	TiW	5000	yes	41.7
15	TiW	2500	yes	28.3
17	TiN	2500	yes	25.1
21	TiN	1300	yes	24.9
14	TiW	5000	no	24.2
16	TiW	2500	no	24.3
18	TiN	2500	no	25.0
22	TiN	1300	no	24.4

8.4.2 Wet Etch Studies of Barrier Metals

The initial samples for wet etch studies in Phase II were prepared using the Innotec V24C sputter deposition system. A number of different barrier layer systems were investigated as shown in Table 30. Test samples were prepared on 100 mm diameter wafers using a 3000 Å thick TiW barrier metal layer and 5000 Å thick gold layer. Some samples were annealed at 300 °C and others left unannealed. The standard resist system and Quintel Q-7000 aligner were used to pattern the bondpad openings on these test samples. Whole wafers were etched in the gold etchant and then in the TiW etchant. The normal gold etch rate of 1200 Å/minute was observed. The TiW etch showed some nonuniformity. Some areas of the wafers cleared in 3 minutes, and others took as long as 5 minutes. Both annealed and unannealed samples behaved similarly. The SEM cross-sections shown in Figures 35 and 36 were taken in both short and long clearing areas for both annealed and unannealed samples.

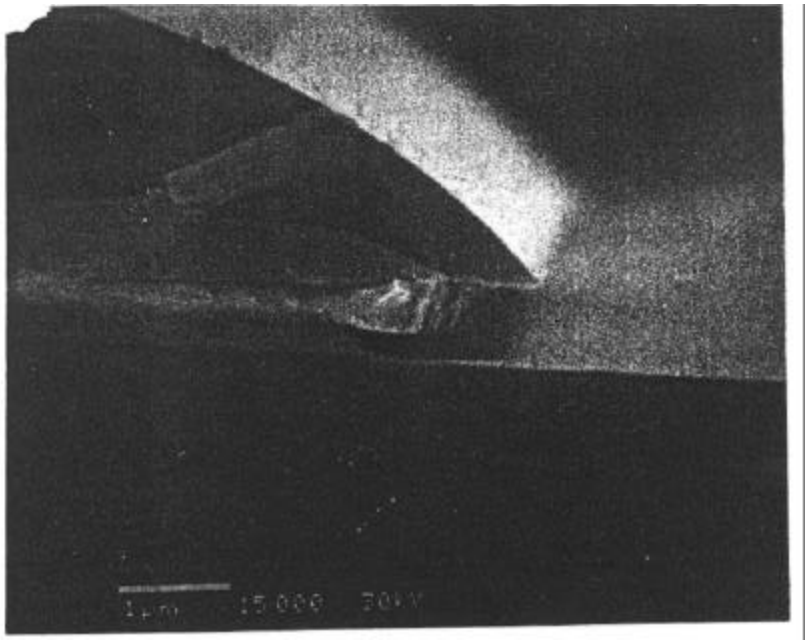


Figure 35. SEM Cross-Section of 300 °C Annealed Wafer After TiW Etch

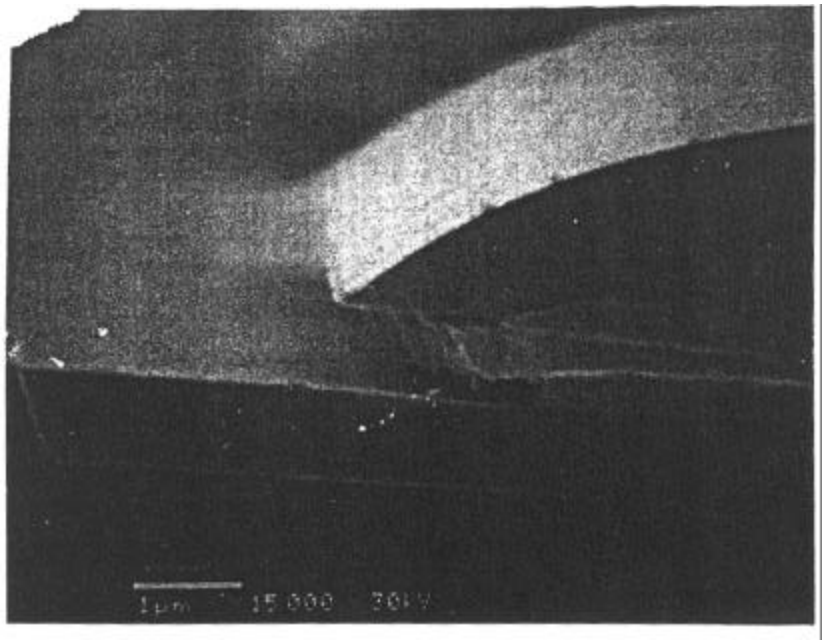


Figure 36. SEM Cross-Section of Unannealed Wafer After TiW Etch

The undercut of the resist from the gold etch is nominally 1-2 μm. The undercut from the TiW etch is similar. No difference in the undercut from the TiW etch was apparent between the first and the last areas to clear on the wafers. In spite of the nonuniformity of the etch, good results for the barrier metal etch were obtained across the entire wafer. The similar behavior of the annealed and unannealed samples suggests that the undercut from the TiW etch is primarily

determined by the deposition conditions. Uncontaminated, leak-free depositions are required to produce acceptable wet etch behavior for TiW barrier metals.

A procedure was adopted in which a control wafer is deposited with the barrier metal and gold for each deposition run to ensure proper wet etch patterning on device wafers. This wafer is patterned and then used as a lead wafer to qualify the wet etch. If unacceptable results are encountered, (i.e., excessive undercut or unusually long etch times) the resist, gold and TiW layers can be stripped and redeposited on the device wafers. The wet etch control wafer qualification is conducted for each wafer lot processed.

Additional 100 mm diameter TiN test wafers were coated with a 400 Å thick TiW adhesion layer and 5000 Å thick gold layer. The gold and TiW were etched in the usual manner. However, attempts to etch the TiN layer in HF/HNO_3 solutions were unsuccessful. Compositions used to etch the previous samples produced no etching, and etchants containing more HF produced excessive undercutting of the gold. In light of the poor results from the TiN etch, the use of a 3000 Å thick TiW film was selected for the ChipSeal barrier metal.

8.4.3 Bondpad Contact Resistance Measurements

During Phase I, some difficulties were encountered in obtaining acceptable bondpad resistance (<100 mO). Upon completion of the high-rel metal patterning, low or nonconducting bondpads were encountered on some of the GEM device wafers. An anneal of the wafers produced acceptable contact resistance. To qualify the bondpad contact resistance, a special set of test wafers was prepared. Blanket Al/Si films were deposited on thermally oxidized wafers. The standard SiO_x and SiC coatings were applied and bondpads etched open. The standard high-rel metal deposition process was used to deposit the metal films and the films were subsequently patterned. The bondpad resistance was measured between two pad openings. The resistance was measured at several locations on the 150 mm test wafers before and after a 300 ºC anneal. The resistance ranged from 1 to 3 ohms prior to the anneal and typically from 50 to 150 milliohms (mΩ) after the anneal. An additional anneal at 350 ºC did not produce any significant bondpad resistance change for these test wafers. It is not understood why the initial contact resistance at the bondpad was so high. Additional work is still needed in this area to better understand and control the metallization materials and process.

8.4.4 High-Rel Metal Deposition Qualification on 150 mm Wafers

Two metal deposition systems were used for Phase II of the program, the Innotec V24C and a Varian 3120 sputter system. Initial qualifications were done with the Innotec system and were qualified on 150 mm wafers. Profilometer measurements were made on TiW patterns on 150 mm wafers to determine the thickness variations across the wafer within a deposition run. For a 2500 Å target thickness, the thickness variation was within ±8 percent. Several wafers were etched individually in the $EDTA/H_2O_2$. Although they all had the same etch rate, 500 Å/minute, as described previously, the wet etch characteristics were erratic and produced unacceptable undercutting.

Metal deposition and qualification was switched to the Varian system, which is equipped with a residual gas analyzer (RGA) for monitoring the background gas contamination levels prior to

deposition. The Varian system produced more consistent depositions and wet etch characteristics compared to the system used in the original work. This highlights the importance of background contamination and its impact on barrier performance. The Varian system was selected for metal deposition on all device wafers processed in Phase II. The composition of the sputter target used for the TiW barrier layer was 0.1 Ti/0.9 W. A quartz crystal thickness monitor determined the thickness and deposition rates of every run.

Two of the 100 mm Varian planetaries were modified to hold four 150 mm wafers. The 150 mm wafers were also moved closer to the sputtering target. The quartz crystal thickness monitor was recalibrated for the 150 mm wafers by direct measurement on test samples.

For qualification, initially 100 mm wafers were coated with TiW/Au in the Varian 3120 S-gun system. Both the TiW and gold were successfully etched with minimal undercut. A similar qualification was done for 150 mm wafers. The etch time reproducibility and uniformity across the wafers were greatly improved. Typical etch times for 3000 Å of TiW is 2 - 3 minutes. Sample wafers were deposited with 3000 Å TiW and 5000 Å gold. The samples were evaluated for film stress and thermal stability up to 400 °C. The results were a considerable improvement over the Phase I results in the Innotec sputtering system where instabilities were observed at 350 ºC heat treatments.

8.4.5 High-Rel Metal Etch on 150 mm Wafers

The wet etch procedure for 150 mm wafers is the same as that used for 100 mm wafers processed in Phase I. Some facility scale-up (larger wet etch baths and wafer carriers) was required to facilitate processing of the live device wafers for Phase II.

The wet etch used for gold consists of 2.5 grams of iodine and 100 grams of potassium iodide dissolved in 1000 ml of H_2O. Typically, the etchant is made up in liter quantities and stored at room temperature until used. The etch is done at room temperature. The etch time for 5000 Å of gold is 5 to 7 minutes. Endpoints are determined by optical inspection after rinsing and drying. The etchant can be reused, but depletion (i.e., longer etch times) is observed with repeated use.

The TiW etch is done with the resist film still intact over the Au. The etchant composition is 2.6 grams of EDTA and 8.4 ml of NH_4OH, in 200 ml of H_20 and 100 ml of H_2O_2. Typically the EDTA and the ammonia are dissolved in the water and stored in gallon containers. The hydrogen peroxide is added at the time the etchant is prepared for use. The etch times for 3000 Å TiW films deposited in the Varian sputter system is typically 2 to 3 minutes. The etch time is quite reproducible. Since the etchant is a clear solution, the TiW removal can be observed during the process. Complete removal is verified with conductivity probes of the wafer surface and optical inspection. The wafer surface is nonconductive after removal of the metal films. The used etchant is discarded after use. Both the Au and TiW wet etches have considerable process margin, and overetching times up to 50 percent appear to present no difficulties. Typical overetch times are 20 percent.

8.4.6 Mask Design and Preparation

During Phase II, photomasks were designed to open the bondpads through the SiO_x/SiC and to define the high-rel metals over the bondpads for each device type. The bondpad layout is

obtained from the device manufacturer and modified to accommodate the ChipSeal design rules. A cross-section schematic of the bondpad configuration is shown in Figure 37. As discussed previously, a 45-55 degree taper is achieved at the edge of the window opening during the dry etch.

The dimensions of the opening, Figure 37, are biased down 11 µm from the original passivation opening, and the high-rel metal covering is biased up 8 µm from the original opening. This provides 19 µm of overlap to provide a seal. The corners of the bondpad opening are chamfered in 5 µm from the edge of the opening.

For Phase II device lots, the streets were opened on all mask designs to facilitate mask alignment to the incoming wafers. Each wafer lot was made by a different supplier, and all had different alignment keys. This approach alleviated the need to add alignment features to the wafers. Where possible, the designs were adjusted to cover the edge with at least a 10 µm strip of SiC extending into the streets.

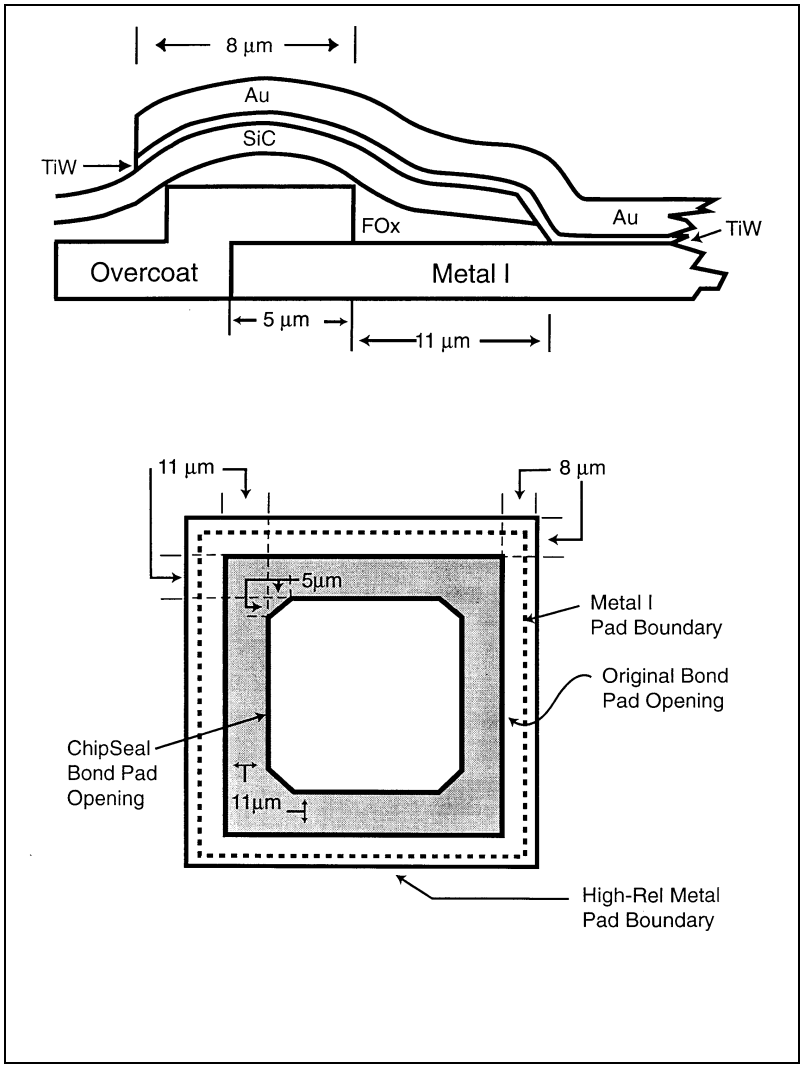


Figure 37. ChipSeal Bondpad Mask Design and Profile Schematic

8.5 *Flip-Chip Processing*

8.5.1 Overview

For six of the device types planned for assembly into the demonstrator modules in Phase II, solder bumping was completed on wafers with and without the ChipSeal dielectric system. The SiC/SiO_x films were deposited at Sarnoff. MCNC then patterned and etched bondpad openings in the dielectric and then processed the wafers through their standard bumping process. A photodefinable polymer, Dow Chemical's Cyclotene 4042-40 (BCB), was deposited on the control wafers that did not receive the ChipSeal coating. All standard bump designs were tailored to obtain 125 µm bump diameters.

8.5.2 SiO_x/SiC Etch Process Development

One of the most critical aspects for successful solder bumping of the ChipSeal wafers is the reactive ion etching of the SiC/SiO_x films. The sidewall slopes of the vias formed by RIE must be tapered so that the step coverage of the UBM will be continuous. Based on work in Phase I, further development of the RIE process was needed to assure that adequate taper was consistently achieved.

A standard MCNC test structure that is routinely used for process verification was used for the RIE process study. The test structure consists of three layers: a base metal (typically Ti/Al), a dielectric layer (SiO_x/SiC) and the solder bumps. Four lots of 25 wafers were produced for the process studies. The 1.2 µm metal layer was deposited and patterned at MCNC, and the wafers were sent to Sarnoff for FOx and 3MS deposition. The test pattern with typical SiO_x/SiC deposition is shown in Figure 38.

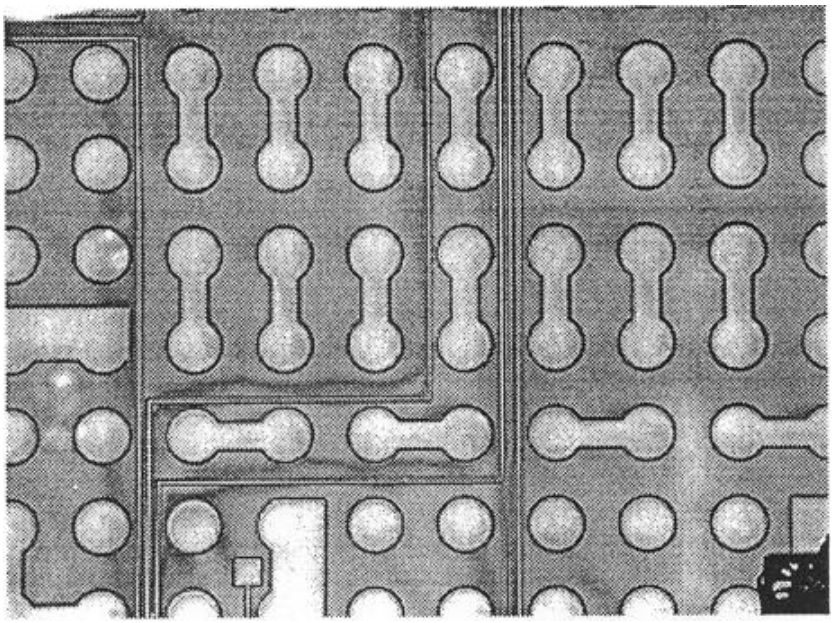


Figure 38. Solder Bump Test Pattern After Successful SiO_x/SiC Deposition

The RIE etch process was developed using a manually loaded single wafer etcher (Plasma Therm 740) to accommodate all of the device wafer sizes (100 - 200 mm) to be processed in Phase II. A high-solids photoresist was chosen to provide thick resist films in order to produce a tapered sidewall in the resist and subsequently in the etched SiC/SiO_x layer during RIE. An 8 µm resist thickness was chosen based on previous work. The benefits of using such a thick resist are that only a fraction of the resist is removed during etch, and the greater thickness allows better control of the slope at the bottom of the feature.

The process developments focused on determining the effect of exposure dose and exposure gap on the sidewall taper in the resist. Exposure gaps of 200-400 µm and dosages of 320-750 mJ/cm^2 were studied. The images obtained at the 300 and 400 µm gap settings were unacceptable because of irregular bottom features. Consequently, exposure dose studies were conducted while maintaining a 200 µm exposure gap. The resulting sidewall angles obtained are shown in Table 31.

Table 31. Average Sidewall Angles Obtained for Different Exposure Doses at 200 µm Exposure Gap

Exposure Dose (mJ/cm^2)	**Sidewall Angle (Degrees)**
320	40
450	50
600	53
750	55

Reactive ion etch conditions were examined as a function of CF_4:O_2 etch gas ratios, gas pressure, power, and bias voltage. Running in the plasma configuration (low DC bias) produced unacceptably low etch rates. Table 32 shows conditions that provided acceptable etch rates and via wall profiles.

Table 32. Process Conditions Producing Acceptable Etch Rates

Condition	**Set Point**
CF_4 Flow Rate:	80 sccm
O_2 Flow Rate:	30 sccm
Pressure:	300 mTorr
Power:	400 W
DC Bias:	280 V

After completion of the process studies, a lot of wafers were run to verify the conditions and characterize the integrity of the bumps produced. The bumps were mechanically tested using a Royce shear tester that produces a shear line 10 µm above the base of the bump. The average shear force was 39.5 grams. This value met the specification for standard bumps fabricated using BCB as the dielectric.

The structure was also electrically tested using Kelvin test structures that were present in the test chip design used for the process development work. The Kelvin test structure allows for a 4-wire measurement of the resistance of the solder within one bump and interfacial resistance between the UBM and underlying aluminum pad. The resistances measured were less than 2 mΩ. These results indicate that the RIE process for the ChipSeal wafers is comparable to the standard bumping process.

8.5.3 Bump Designs

Early analysis of the device and module designs revealed that the use of 125 µm bumps would not be possible on the high I/O devices without some type of redistribution. Traditional redistribution entails the use of a patterned aluminum layer to move the I/O pads to positions where adequate space is available. To accomplish this, an additional mask step is required, which not only adds cost but also requires the application of an additional layer of BCB on top of the ChipSeal dielectric. This additional layer would have made it difficult to quantify the contribution of the ChipSeal coating to any reliability improvements that may be seen during the subsequent reliability testing. Consequently, MCNC's newly developed Single Mask Redistribution (SMR) process was used.

The SMR process eliminates one mask level for a design that requires redistribution by performing the redistribution of I/Os within the solder layer. Although routinely used for solder bumping commercial parts, the use of the SMR process has been limited to only a few designs. In order to minimize the risk for the designs required for the Phase II devices, a test mask was designed and fabricated for all of the potential designs for all the device types to be flip-chip mounted in Phase II. The test wafers were bumped using the SMR process, and the designs were evaluated for form, separation, and reproduction. Test design examples included reduced diameter bumps (100 µm), elongated bumps (100 by 300 µm), and an alternating offset array using 150 µm long connection lines (Figures 39-41). Following the test wafer evaluation, the most suitable designs for each device type were mutually chosen by MCNC and Rockwell.

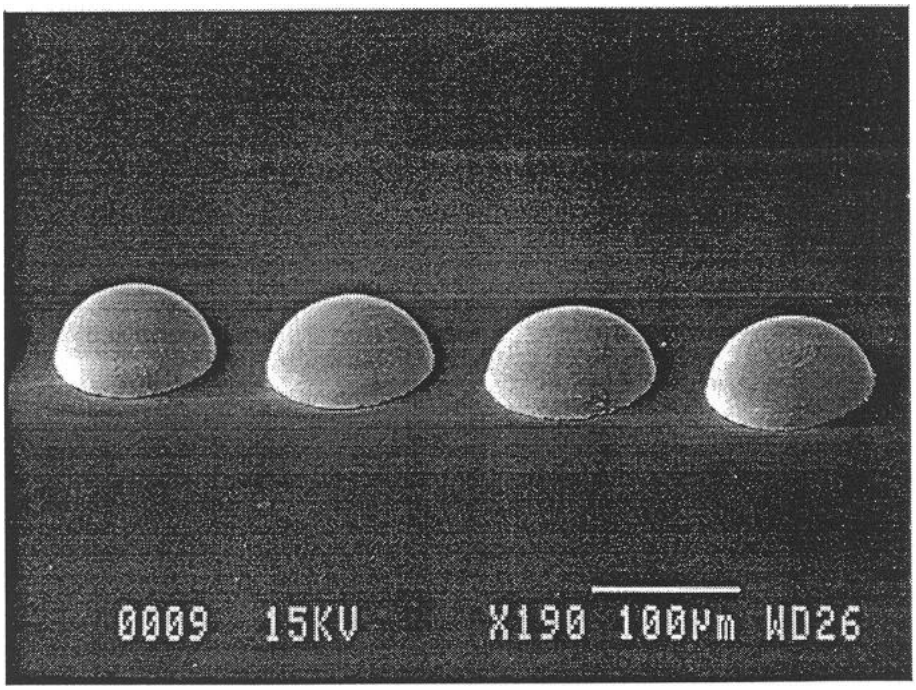


Figure 39. Photomicrograph of 100 µm Diameter Solder Bumps

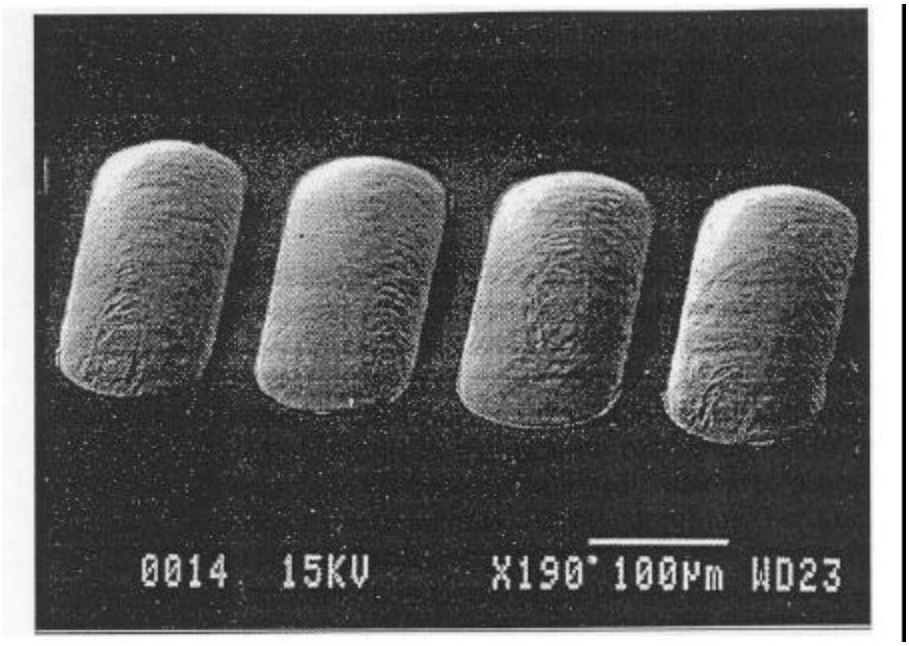


Figure 40. Photomicrograph of 100 by 300 µm Bump Designs

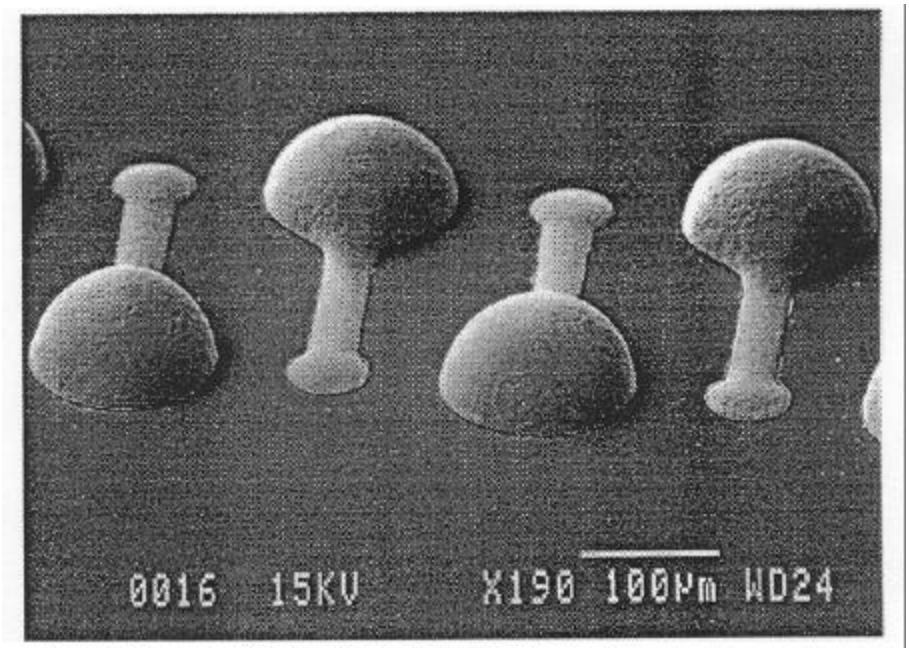


Figure 41. Photomicrograph of SMR Bump Designs

All of the designs that could be fabricated using standard 125 µm diameter bumps were designed as such. Those devices having high I/O count and narrow pad pitch were designed using the alternating offset and, in one design, a fan redistribution of corner I/O. The fan distribution required the use of a slightly modified SMR process to assure uniform bump heights, since some fairly long line lengths were required (1400 µm). The coplanarity of the bumps using the modified process were within a few microns.

9. ChipSeal Process Assessment for Commercial/Proprietary Device Wafers

The objective of Phase II is to demonstrate the compatibility of the ChipSeal process with a variety of commercial device types. Approximately 100 wafers of 6 different commercial and four proprietary ASIC device types were processed. The device types, number of wafers, and characteristics are summarized in Table 33.

9.1 *Device Selection, Process and Evaluation Plan*

The six commercial device types were selected jointly with Rockwell-Collins for evaluation in demonstrator MCMs. The wafers for use in the modules were purchased through Chip Supply, Inc. Die sizes ranged from 71 by 125 mils to nearly 400 mils per side and the bondpad count ranged from 10 to over 200 for the largest die. In all instances the bondpads were normal size (100 µm square), but for the die having the largest I/O counts (the digital signal processor (DSP) and microprocessor), the spacing between pads was reduced. The analog devices (Opamp and amplifier) were selected for signal conditioning functions for distributed aircraft control system sensors. The DSP, microprocessor, and the memory devices were selected for their specific functions in a GPS based navigation/guidance system.

The proprietary devices were supplied by either government agencies or IC manufacturers.

Table 33. Description of IC Types

	Commercial Devices						*Proprietary Devices*			
IC Type	Si Analog	Si Analog	Si Digital	Si Digital	Si Digital	Si Digital	Si Digital	Si Digital	SOS Digital	Si Test Chip
Function	Opamp	Amplifier	DSP	Micro-processor	SRAM	Flash	Multiplexer	Controller	Shift Register	Corrosion Test Track
Wafer Dia (mm)	100	100	150	200	150	150	150	100	100	150
Die size (in.)	.108 x .125	.071 x .125	.393 x .395	.176 x .181	.139 x .389	.170 x .185	.287 x .395	.420 x .195	.300 x .300	.250 x .250
Number I/O	14	10	208	93	33	30	208	72	40	40
Wafer Thickness (in.)	0.022	0.022	0.0195	0.029	0.013	0.02	0.022	0.022	0.026	0.022
Number processed	7	7	21	10	14	6	23	6	14	6
Process Configurations										
Control	1	1	4	2	2		2		8	
CS+GP	2	2	6		6		21	2+2+2	14	6
CS+GB			3	4	2	2				
CS+SB	2	2	4	2	2	2				
SB Control	2	2	4	2	2	2				

CS = ChipSeal GB = Gold Bumped GP = Gold Pad SB = Solder Bump

The process and evaluation plan for the MCM demonstrator devices is shown in Figure 42. The devices (wafers) were divided into the following four groups for processing:

- A wire bond control group that received no processing.
- A ChipSeal processed group intended for standard wire bond interconnect.
- A ChipSeal processed group intended for flip-chip (solder bump) interconnect.
- A solder bump control group.

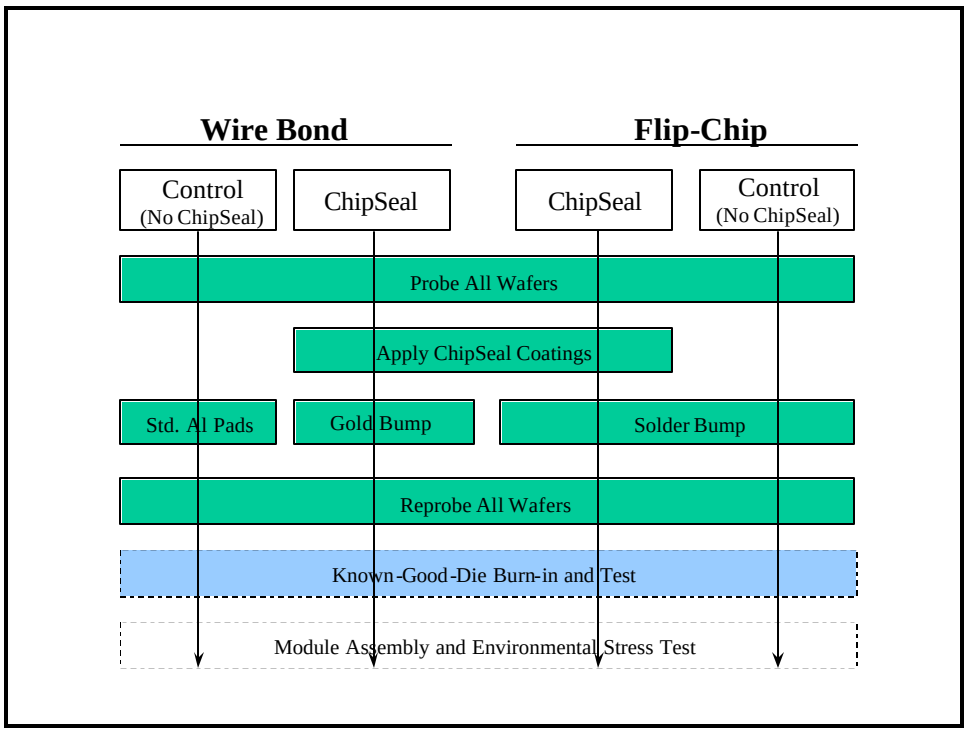


Figure 42. Wafer Process and Evaluation Plan for MCM Demonstrator

Those designated to receive ChipSeal coatings were processed at Sarnoff for application of the dielectric coatings and opening of the bondpads. The wafer groups were then further subdivided to receive the appropriate metallization. Those to be used in the MCM module evaluations with wire bond interconnects were gold bumped at a commercial bumping service. Gold bumps were used to provide sufficient pad height for subsequent KGD testing using temporary tab bonding techniques [12]. Those intended for module testing in the flip-chip configuration were metallized at MCNC. Before and after wafer probe, yield data was used to assess the effects of the processing. After probe testing, selected wafers were diced and sorted, and a specific number of die of each device type were assembled on temporary carriers for burn-in and KGD evaluation. The purpose of this evaluation was to eliminate from module assembly those die prone to early failure. Finally, test modules were assembled for subsequent environmental stress tests using bare die with wire bond interconnections or flip-chip interconnections. The use of organic encapsulants or underfills to protect the interconnections was also evaluated.

The wafer process routing used for this evaluation is shown in Figure 43. The wafers used for the modules were shipped directly to Chip Supply for initial inspection and testing (wafer probe). The wafers not involved in the module demonstration were shipped to Dow Corning to arrange their processing because of the sensitive nature of some of the device types. It was requested that the manufacturers not mark or probe the wafers before shipment since the wafers would be going through additional thin film deposition and metallization processes. Residues from ink marks used to identify nonfunctioning die could contaminate or jeopardize the integrity of the ChipSeal coatings, and probe marks on the aluminum bondpads could prevent complete coverage of the high-rel metallization. However, this request could not always be honored because operational routines or policies in some of the fabs require wafer level testing of all product before release. As part of the procurement, each of the suppliers made available the

appropriate device and wafer layout data files that would allow fabrication of bondpad and metallization masks. The data files were supplied to Sarnoff and MCNC for subsequent processing.

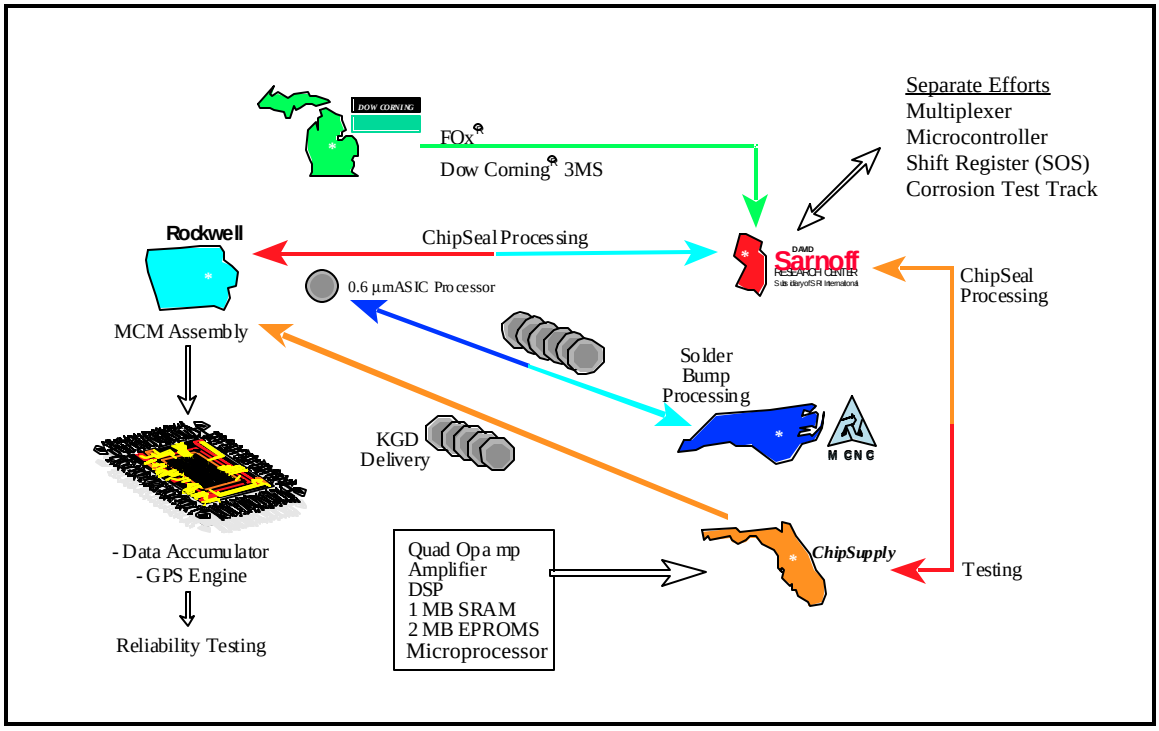


Figure 43. ChipSeal Wafer Process Routing

The methods used for process compatibility assessment is summarized in Table 34.

Table 34. Methods Used to Assess Wafer Yield Impact

Device	Opamp	Amplifier	DSP	Micro-Processor	Memory SRAM	Memory Flash	Multiplexer	Controller	Shift Register	Corrosion Test Track
Predelivery wafer probe at IC Supplier	Yes	Yes	Yes	No	Yes	No	Yes	Yes	No	No
1st Probe at CSI before ChipSeal or flip-chip processing	Yes	Yes	No	Yes	Yes	No	No	No	No	No
2nd Probe at CSI after ChipSeal or flip-chip processing	Yes	Yes	No	Yes	Yes	No	No	No	No	No
Returned to supplier for final wafer probe after ChipSeal or flip-chip processing	No	No	Yes	No	No	Yes	Yes	Yes	Yes	No
Method of yield impact assessment	Compare 1st probe to 2nd probe	Compare 1st probe to 2nd probe	Compare pre-delivery to 2nd probe	Compare 1st probe to 2nd probe	Compare 1st probe to 2nd probe	Compare final to historical	Compare 1st probe to 2nd probe	Compare 1st probe to 2nd probe	Compare control and processed at final probe	Special test methods used to assess corrosion

Upon receipt, Chip Supply visually inspected all wafers and probed a fixed percentage (≥ 20 percent) of die on each wafer to determine an incoming yield. The die positions for the probe were randomly selected from each quadrant of the wafer so as to be representative of the whole wafer. Die locations and test results were logged for each wafer and the same die were probed again after processing to determine the effects of the processing on functional device yield, i.e., process compatibility. Thus, for the device types not probed by the manufacturer, a significant number of die on each wafer would retain pristine or unmarked bondpads for subsequent high-rel metallization or solder bumping. At least one wafer of each device type was held as a probe and reliability test control and did not receive additional processing. After inspection and testing, the wafers designated for ChipSeal processing were sent to Sarnoff for thin film coating. A few wafers were metallized by Sarnoff, but the majority were metallized by a commercial wafer bumping service company, Aptos. Gold bumps were required for subsequent KGD testing before module assembly. Those intended for module assembly in the flip-chip configuration were solder bumped at MCNC. This process flow is shown in Figure 44. With one exception, all processed wafers (commercial products) were returned to Chip Supply for final probe, inspection and dicing. The functional die was sent to Rockwell for assembly on temporary carriers for the KGD testing and subsequent module assembly and testing.

9.2 *Wafer Processing*

Ten separate device wafer lots were processed with the ChipSeal hermetic coatings. Nine of the lots, all 100 and 150 mm wafers, were processed at Sarnoff; the tenth lot, 200 mm wafers, received split processing due to size limitations at Sarnoff. For the 200 mm wafers, the spin-on FOx coating was applied in a high volume commercial 200 mm IC fabrication facility currently using the FOx materials as an interlayer dielectric; the plasma-SiC application was conducted at Dow Corning's Application Center, and the wafers were patterned and etched at MCNC to open the bondpads. Those wafers designated for wire bond were metallized (gold bumped) at the commercial bumping service.

9.2.1 Mask Design

Photomasks were designed to open the bondpads through the SiO_x and SiC coatings and to define the high-rel metals over the bondpads. This process involved obtaining the bondpad layout from the manufacturer and then modifying the layout to accommodate the ChipSeal design rules. Figure 32 shows a cross-sectional schematic of a typical opening design. The bondpad opening is biased down 11 µm per side from the original bondpad opening, and the high-rel metal is biased up 8 µm from the new via opening. The corners of the ChipSeal opening were chamfered 5 µm to reduce corner stresses.

Each device lot was made by a different semiconductor manufacturer and each had their own unique alignment keys for wafer processing. To provide a consistent approach for mask alignment without adding alignment keys to the wafers, the streets were opened on all device lots. This facilitated consistent alignment of the high-rel metal to the device bondpads. A 10 µm overlap of the SiC coating into the street was incorporated into the design to provide a seal at the edge of the die.

9.2.2 Lot Process Histories

The individual lot processing histories are summarized in Volume 2. The summary includes processing parameters and/or exceptions specific to each device type.

9.2.3 Wafer Defects and Processing Issues

A number of different types of defects were observed on incoming wafers and after ChipSeal processing. Many of the wafers had not been packaged properly for reentry into a cleanroom environment. Often filter paper covers were included in the wafer carriers. This generated additional particulate defects in the films that were not removed in routine cleaning steps prior to film deposition. In addition, many of the wafer sets had been ink dot marked after probe testing by the original device manufacturer. In some instances, solvent cleaning procedures easily removed these, but in others, the inks left non-removable residues even after oxygen plasma treatments that generated additional particulates during the SiC plasma deposition. This not only contaminated the subject wafers but also contaminated others that were sharing the same deposition run.

Approximately half of the incoming wafers had been probe tested prior to receipt. In some instances, the bondpads were heavily gouged or the passivation was damaged by misalignment of the probe. In others, the marks were well centered and relatively innocuous. However, any probe marks can generate defects during the metallization, particularly the uniform coverage of the TiW diffusion barrier, which can negatively impact final reliability of the contact. For those wafers that were not probed by the manufacturer, only a designated sample of die sites were probed before processing to establish their initial yields.

It must be pointed out that it was initially requested that the wafers not be probe tested or marked at the time of manufacture. However, because of the rigid routines established in the manufacture of commercial devices, this could not always be accommodated. Consequently, diligence must be exercised in knowing what procedures were used in the manufacture of a particular device and establishing appropriate corrective methods.

9.3 *ChipSeal Process Compatibility Assessment*

The prime objective of the Phase II effort was to determine if the additional ChipSeal materials and processes were compatible with a variety of IC device types as evidenced by the effects on product yield. The methodology used compared wafer probe yields before and after processing. Table 34 shows the method of wafer probe evaluation that was used for each wafer type (determined separately by each wafer fabricator). Six of the wafer types were given a normal wafer probe evaluation by the manufacturer prior to delivery. Four of the commercial devices types were probed at Chip Supply, Inc., both before and after ChipSeal processing. Two of the commercial and all of the proprietary device types were returned to the supplier for final probe. A comparison of the pre- and post-processing wafer yields is used to assess the impact of the ChipSeal process. It should be noted that some wafer types received two or more separate probe steps prior to processing. Also, it should be noted that the ChipSeal process was not optimized for each device type. Rather, an arbitrary set of process parameters was used generally across the board. The following summarizes the probe results for the various processes used. The

absolute wafer yield information is considered company proprietary. Thus, only the pre- to post-process differential yields are reported.

9.3.1 Experimental Procedure

For the commercial devices, approximately 20 percent of the die on each wafer were probed by Chip Supply prior to processing. The die were selected at random from each quadrant of the wafer. The same die was reprobed after processing. For the proprietary devices, the initial and final probes were conducted by the manufacturer. The exceptions to this procedure are noted in Table 34.

At least one wafer from each group was designated as the control wafer and received no additional processing. A minimum of four wafers received the ChipSeal hermetic coatings (two for each type of metallization). These wafers were then etched to open the bondpads and were gold bumped or solder bumped. Also, two solder bump control wafers were prepared that did not receive the ChipSeal coatings. The process configurations are listed in Table 35, and the general process flow is shown in the Figure 42. The same die on each wafer was re-probed after processing to assess process/device compatibility as evidenced by the change in yield.

9.3.2 Assessment of Wafer Probe Repeatability

The control wafers (standard passivation and standard aluminum pads) were probed along with the processed wafers (pre- and post-processing) to assess the variability in the probe process itself. Under ideal conditions, the first and second probe results for the control wafers should be identical. For the 12 control wafers that were double probed in the program, the repeatability is considered quite good (only 87 devices tested differently out of a total 1906 devices probed constituting 4.6 percent. But only three wafers gave identical results.

9.3.3 Impact on Yield of the ChipSeal Hermetic Coating Process

A nonproprietary version of the wafer probe results is shown in Table 35. (i.e. Only differential results are shown for the number of devices probed; absolute yields are company proprietary.) The results are quite encouraging. For the first five commercial device types listed, of particular note is the small number or percentage of die sites that changed after ChipSeal processing. Relative to the change observed for the control samples, in most instances, the change observed for the processed samples are insignificant and are considered to be within the variability of the probe process itself.

Table 35. Yield and Process Compatibility Summary by IC Type and Process

	Commercial Devices						*Proprietary Devices*			
IC Type	Analog	Analog	Digital	Digital	Digital	Digital	Digital	Digital	Digital	
Device Type	Opamp	Amplifier	DSP	Microprocessor	SRAM	Flash	Multiplexer	Controller	Shift Register	Corrosion Test Track
Wafer Dia (mm)	100	100	150	200	150	150	150	100	100	150
Die size (in.)	.108 x .125	.071 x .125	.393 x .395	.176 x .181	.139 x .389	.170 x .185	.287 x .395	.420 x .195	.300 x .300	.250 x .250
Number I/O	14	10	208	93	33	30	208	72	40	40
Average Net Change by Process (No. of Die/wafer)										
Process										
Control	+4	-2	+4.3	+.5	0.0	NA	0	TBD	0	NA
CS / Gold Bump	+2	-1.5	-10.5	-2.8	-4.0	-347	NA	NA	3.3	NA
CS / Solder Bump	-1.5	-18	-.5	-19	-1.0	NA	NA	NA	NA	NA
Solder Bump Control	-3.5	-24	+8.7	-6.5	-0.5	16	NA	NA	NA	NA
CS / Gold Pad	--	--	-5.3	--	+0.3	--	-176	TBD	--	NA
Average Net Change by Process (% of Die Probed/Wafer)										
Process										
Control	+3.3	-1.0	+3.1	+0.2	0.0	NA	0	TBD	0	NA
CS / Gold Bump	+0.8	-0.7	-7.8	-1.0	-3.3	-50.9	NA	NA	5.0	NA
CS / Solder Bump	-1.2	-8.7	-0.4	-7.4	-1.6	NA	NA	NA	NA	NA
Solder Bump Control	-3.2	-11.9	+6.5	-2.5	-1.0	-2.7	NA	NA	NA	NA
CS / Gold Pad	--	--	-3.9	--	+0.5	--	-83.2	TBD	--	NA
Compatibility Summary Wafer Yield Change	Three increased, one unchanged, two decreased	One increased six decreased	Seven increased, two unchanged, nine decreased	Two increased, two unchanged, six decreased	One increased, nine unchanged, three decreased	Three indeterminate, three decreased	All decreased	Four decreased	Thirteen increased, one indeterminate	NA

9.4 *Individual Device Results and Discussion*

9.4.1 Commercial Devices

9.4.1.1 ***Operational Amplifier Device (Opamp) Results***

Figure 44 shows the result (net change) for the operational amplifier device wafers. A total of 856 devices on seven wafers were probed before and after processing. Of these, 823 (96 percent) gave the same result after processing as before. Of the 4 percent that gave different results, the following observations were made:

- On the wafers that received the ChipSeal gold bump process, three devices changed from fail to pass (recovered) and one device changed from pass to fail.
- On wafers that received ChipSeal and flip-chip solder bumping, three devices failed and none recovered.
- On wafers that received only solder bumping (flip-chip controls), three devices recovered and eighteen devices failed.
- Five devices on the control wafer recovered.

Only the flip-chip failures appear to be significant, and since they occurred on only one wafer, they are suspected to be related to formation defects in the solder balls that prevented adequate

probe contact. All other changes appear to be within the uncertainty of wafer probe repeatability. Opamps are linear devices whose characteristics are known to be extremely sensitive to temperature, stress, moisture and ionic contamination which can cause shifts in their operating characteristics that constitute device failure. It is significant that for this device type, virtually no failures are attributable to the ChipSeal processing.

There is no yield degradation or change in electrical performance attributable to the ChipSeal hermetic coating process.

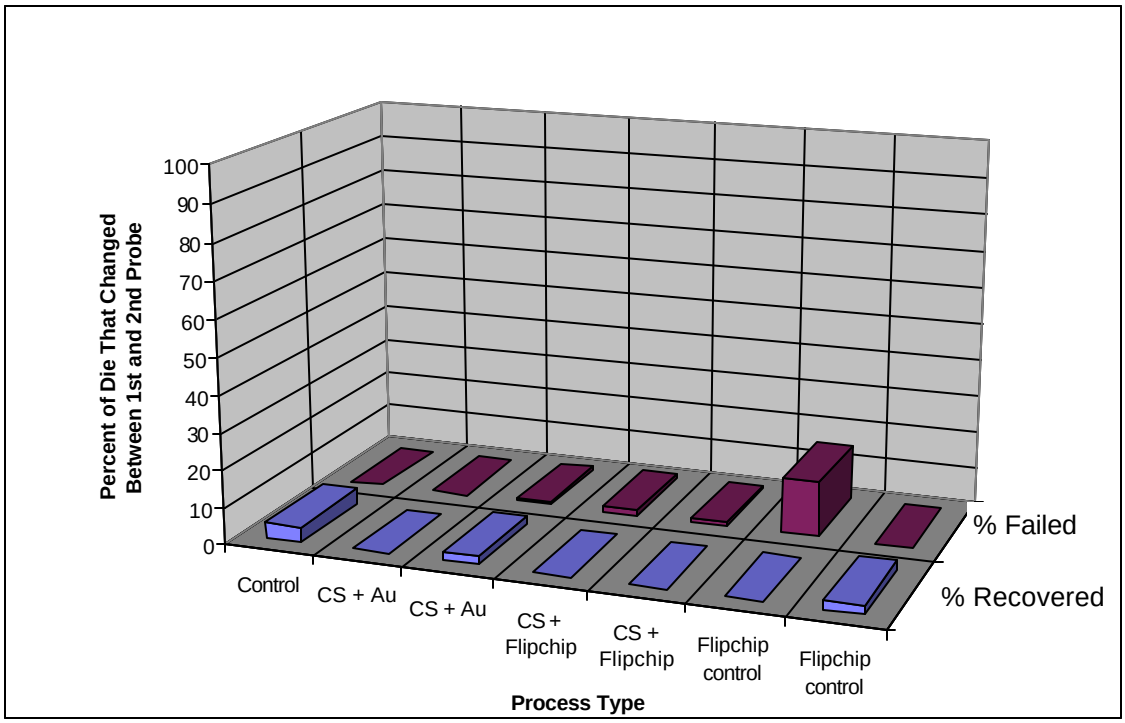


Figure 44. Impact of ChipSeal Processing on Yield of Opamp Device Wafers

9.4.1.2 ***Differential Amplifier Device (Amplifier) Results***

The net effect on yields for the amplifier devices is shown in Figure 45. A total of 1440 devices on seven wafers were probed before and after ChipSeal and flip-chip processing. Of these devices, 1331 (92 percent) gave the same result after processing as before. Of the 8 percent that gave different results, the following observations were made:

- On wafers that received ChipSeal gold bump processing, two devices recovered and six failed.
- On wafers that received both ChipSeal and flip-chip processing, one device recovered and thirty-eight failed.
- On wafers that received only solder bumping, eight devices recovered and fifty-one failed.
- On the control wafer, three devices failed.

Again, the only significant trend appears to be the loss of some flip-chip devices. This again correlates with variability in bump formation at sites that initially exhibited deep probe marks, thus resulting in irregularly formed bumps and subsequent probe contact faults. Amplifiers are linear devices whose characteristics are known to be extremely sensitive to temperature, stress, moisture and ionic contamination that can cause shifts in their operating characteristics that constitute device failure. It is significant that for this device type, virtually no failures are attributable to the ChipSeal processing.

No yield loss or change in electrical performance is attributable to the ChipSeal hermetic coating process.

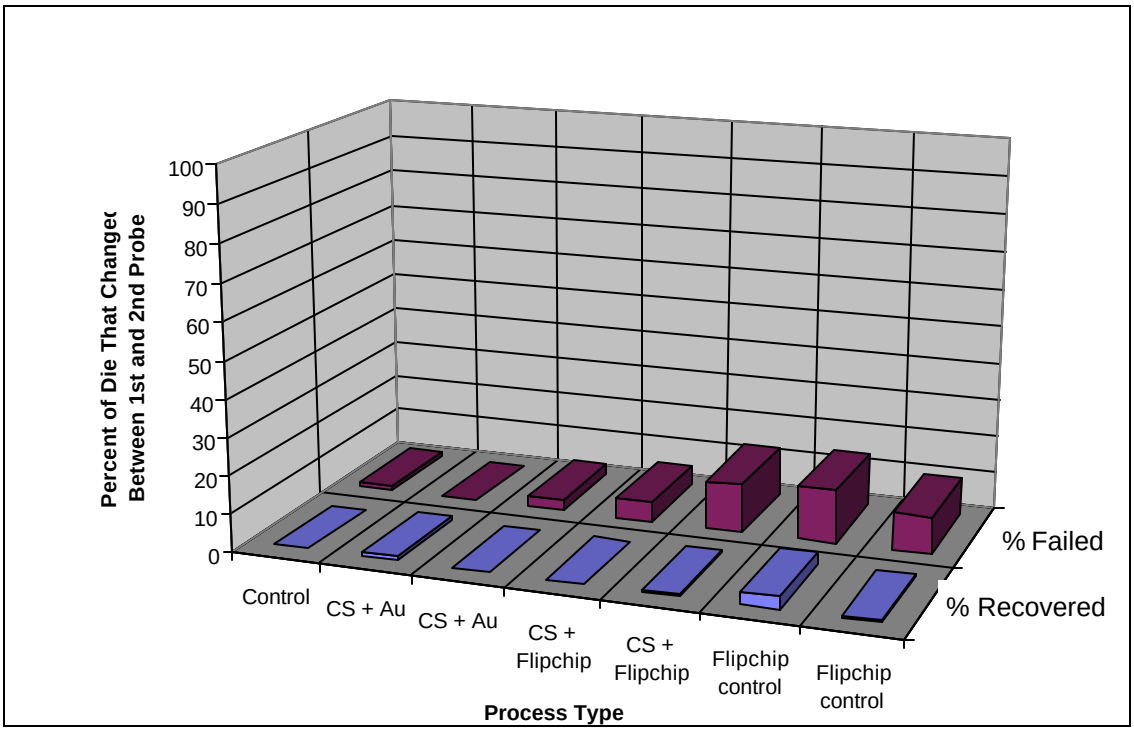


Figure 45. Impact of ChipSeal Procesing on Yield of Amplifier Device Wafers

9.4.1.3 ***DSP Results***

The results for the DSP are shown graphically in Figure 46. A total of 2430 devices on 18 wafers were probed before and after ChipSeal and flip-chip processing. Of these, 2128 (87.6 percent) gave the same results after processing as before. Of the 12.4 percent that gave different results, the following observations were made:

- On the wafers that received only the ChipSeal gold bump processing, 31 devices changed from fail to pass (recovered) and 84 devices changed from pass to fail - a total change of 115 devices in 1080 devices probed, or 10.7 percent.
- On wafers that received ChipSeal and flip-chip processing, 16 devices failed and 17 devices recovered - a total change of 33 devices in 270 probed or 12.2 percent.

- On wafers that received only flip-chip solder bumping, 60 devices recovered and 25 devices failed - a total change of 85 devices in 540 probed or 15.7 percent.
- On the control wafers 43 devices recovered and 26 devices failed - a total change of 69 devices in 540 probed or 12.8 percent.

No significant change in device performance is a result of the ChipSeal processing.

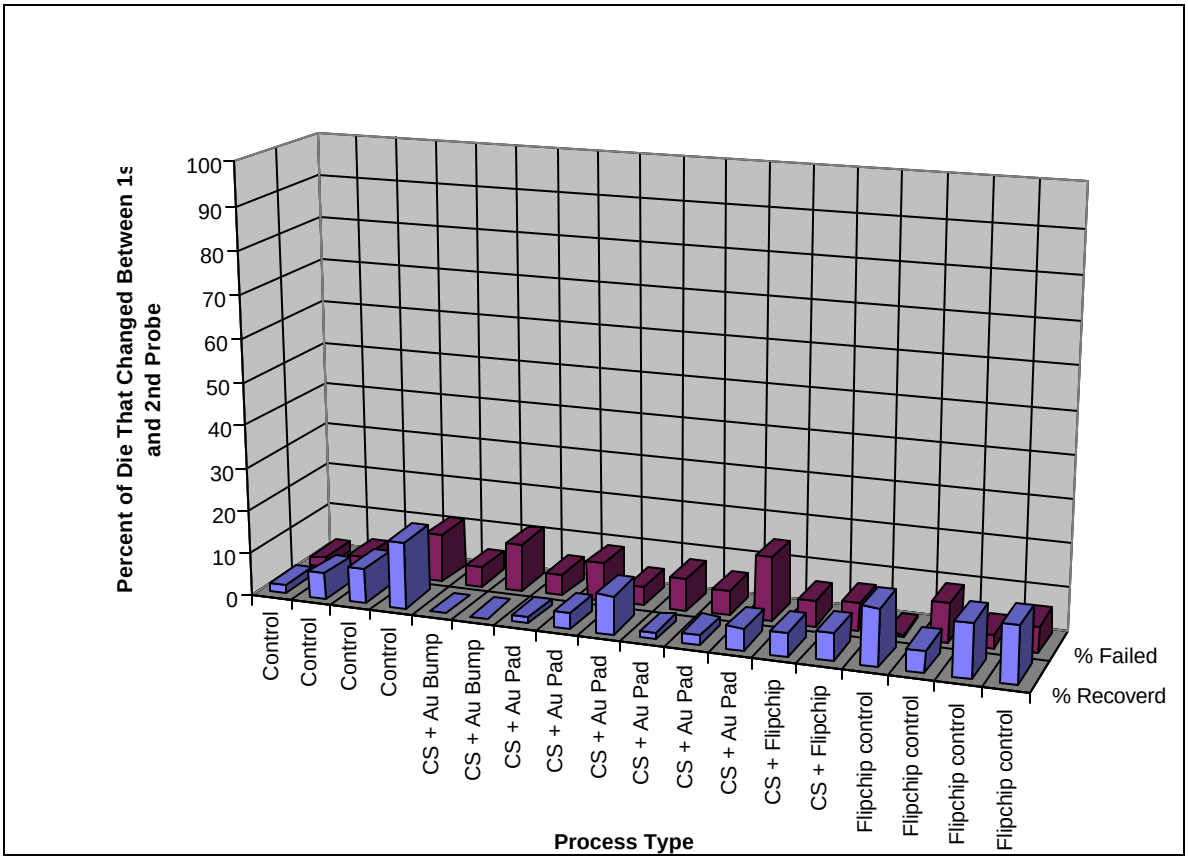


Figure 46. Impact of ChipSeal Processing on Yield of DSP Device Wafers

This data shows a level of variability that should be expected for high I/O count devices. The percent total change for the ChipSeal processed devices is less than the control devices. Flip-chip processing appeared to actually improve yield (net positive change). However, it is more likely that the soft solder bumps introduced less probe contact resistance at the second probe than the oxidized aluminum pads at first probe. The ChipSeal coated devices showed a net loss of 53 devices out of 1080 devices that were double probed. This 5 percent variation is less than the repeatability for the control devices. The variability observed for the control wafers is reflected in all combinations of flip-chip and ChipSeal processing.

9.4.1.4 ***Microprocessor Device Results***

The results for the microprocessor are shown graphically in Figure 47. A total of 2570 devices on 10 wafers were probed before and after ChipSeal and flip-chip processing. Of these, 2484

(96.7 percent) gave the same results after processing as before. Of the 3 percent that gave different results, the following observations were made:

- On wafers that received ChipSeal/gold bump processing, 7 devices changed from fail to pass (recovered) and 14 devices changed from pass to fail. A total change of 2.0 percent (21 devices in 1028 probed).
- On wafers that received both ChipSeal and flip-chip solder bump processing, 3 devices recovered and 32 devices failed. A total change of 6.8 percent (35 devices in 514 probed).
- On wafers that received only flip-chip processing (solder bump controls), 6 devices recovered and 16 devices failed. A total change of 4.3 percent (22 devices in 514 probed).
- On the control wafers, 7 devices recovered and 1 device failed, for a total change of 1.6 percent.

Virtually no failures are attributable to the ChipSeal processing.

The two wafers that had both ChipSeal and flip-chip processing showed the highest net yield loss (5.6 percent), but considering the higher probe variability for the solder bumped wafers in general (5.5 percent), the result is considered within the limits of probe repeatability.

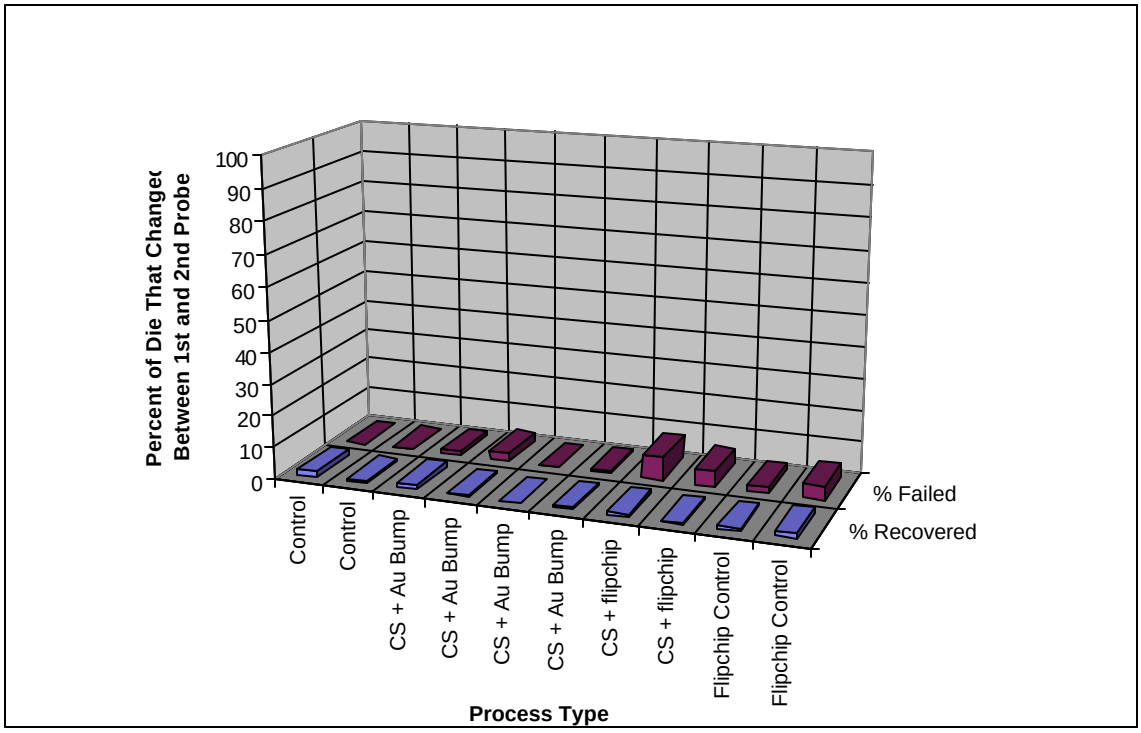


Figure 47. Impact of ChipSeal Processing on Yield of Microprocessor Device Wafers

9.4.1.5 ***SRAM Device Results***

The results for the SRAM are shown graphically in Figure 48. A total of 685 devices on 13 wafers were probed before and after ChipSeal and flip-chip processing. Of these, 662 (96.6

percent) gave the same results after processing as before. Of the 3 percent that gave different results, the following observations were made:

- On the 8 wafers that received ChipSeal bold bump or thin gold pad processing, 5 devices changed from fail to pass (recovered) and 16 devices changed from pass to fail.
- The single wafer that received both ChipSeal and flip-chip solder bumping had duplicate probe results before and after processing (i.e., no change).
- On the two wafers that received only flip-chip solder bumping, both had duplicate probe results before and after processing (i.e., no change).
- On the control wafers, two devices failed and none recovered.

Virtually no failures occurred as a result of the ChipSeal processing.

The largest change observed for this wafer set is the net loss of 11 die on the ChipSeal coated wafers. It is important to note that 9 of the 11 were on a broken wafer and only 36 of the original 55 die sites could be probed the second time. Damage associated with the fracture could have contributed to a majority of the failures. Nevertheless, out of 412 such devices, the net 11 failures represents less than 3 percent change, which is considered below the limits of probe repeatability.

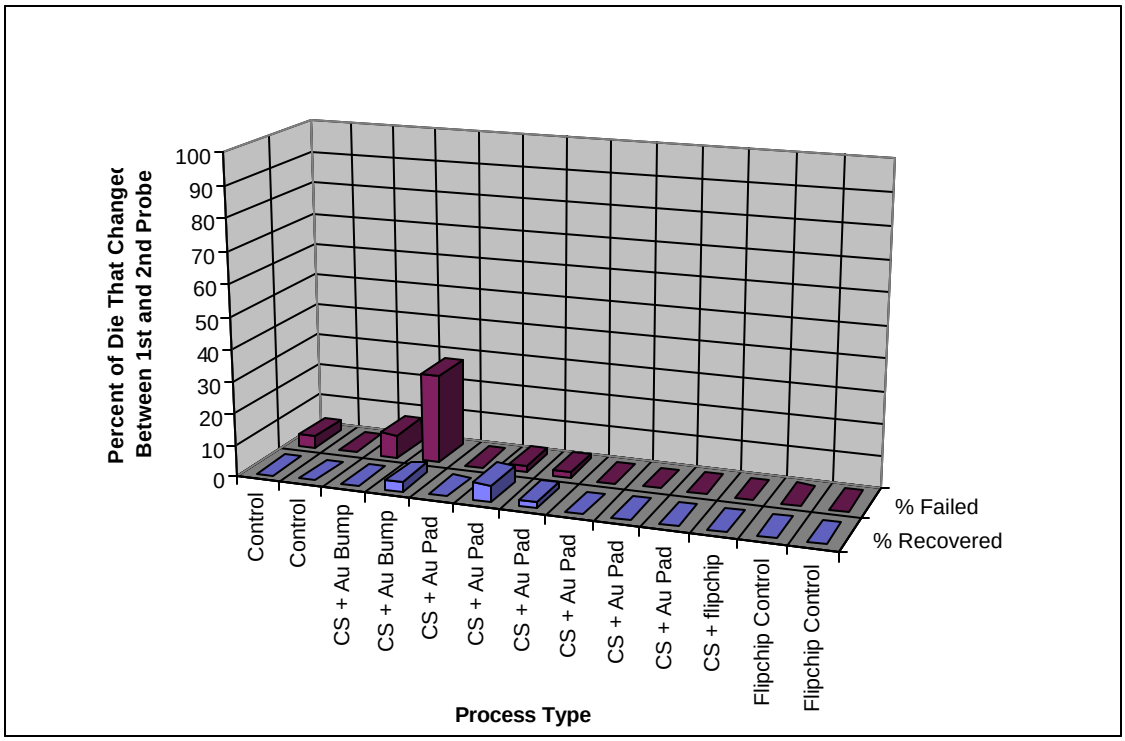


Figure 48. Impact of ChipSeal Processing on Yield of SRAM Device Wafers

9.4.1.6 ***Flash Memory Device Results***

The results for the flash memory devices are not comparable because of the different assessment procedure used. These wafers were tested by the manufacturer. One control wafer was probed

along with the processed wafers. Thus, the repeatability of the probe process for this device could not be assessed. One ChipSeal gold bump wafer was broken at final probe. The yield for the second showed a significant decline from normal, providing only 65 good die. The ChipSeal solder bump wafers tested completely nonfunctional at final probe yet isolated die from those wafers were functional and were used in subsequent assembly tests. A breakdown by failure type was not provided but most were opens.

The results are considered more indicative of probe errors than process related failures and are inconclusive for this study.

9.4.2 Proprietary Devices

9.4.2.1 ***Multiplexer Device Type***

Seventeen wafers in this set received standard ChipSeal processing, including thin film gold metallization. Two additional wafers were held in reserve as controls. After processing, a significant reduction in yield (45 percent) was reported. A reprobe of the controls and selected process wafers indicated no change for either group. Seventy-nine percent of the failures were due to open circuits. Suspecting a contact or metallization issue, selected wafers were reannealed. A small improvement (~6 percent) was observed. Attempts to define the location of the failures by stripping the secondary metallization and reprobing on the original bondpads were unsuccessful. The cause of the yield reduction is unclear. Wafer lots of the same device had been processed previously with minimal impact. This was the first wafer lot processed in this study and process parameters were still undergoing some adjustments. However, there are no indications that processing errors contributed to the yield impact. Also, wafer lots of the same device have been processed since this effort, with minimal losses.

9.4.2.2 ***Shift Register Device Type***

Fourteen wafers were received for processing and eight were held by the manufacturer as controls. It is important to note that these were SOS devices. This device type was not originally intended to be included within the program but were included when the need and opportunity arose because of the extra challenge represented. Different processing parameters were required because of the different heat capacity and conductivity of the substrate. The manufacturer also requested that these wafers be processed with gold bumps.

The controls and process wafers were probed only once at completion of the processing. Individual wafer results were not reported, only average values for each group were reported. The wafers had an average increase in yield of 3.3 die per wafer, or a total of 43 die for the lot. The increase is attributed to improved contact at probe as the result of the gold metallization.

9.4.2.3 ***Corrosion Test Track Wafers***

These wafers were processed in support of the Rockwell Impedance Spectroscopy Program. Their performance is reported elsewhere. Yield measurements are not applicable.

9.4.3 General Yield Considerations

The previous discussions for most of the individual device types have concluded that there is no inherent yield degradation as a result of various process exposures within the ChipSeal coating operations or the flip-chip solder bumping process. Again, it should be kept in mind that no process optimization was conducted for any device type; only generalized parameters were used. However, the following related yield issues need to be considered:

- Device loss due to probe mark damage
- Device loss due to contamination
- Device loss due to wafer breakage.

9.4.3.1 ***Probe Mark Damage***

The presence of deep or multiple probe marks on the original aluminum bondpads can interfere with the correct formation of the final I/O metallization. In some cases deep or multiple probe marks were observed to cause defective gold pad or solder bump formation on devices that subsequently exhibited contact failures. A few percent of the devices from some wafers were rejected at visual inspection for use in subsequent assembly evaluations because of probe related defects. The preferred approach is to delay probing until completion of the ChipSeal and flip-chip processing to eliminate this type of yield loss.

9.4.3.2 ***Contamination-Induced Yield Loss***

Several wafer types in this program had been delivered with ink dot markings from the manufacturer's probe / die sort processes. The ink markings can become contaminants for the ChipSeal thin film deposition processes. In some cases the markings could not be completely removed by standard cleaning procedures. Residues remained that caused defects in the coatings or at the bondpads after processing. Again, a few percent of the devices were rejected at visual sort for this type of defect. The preferred approach to delay probing and marking until after the processing is complete.

9.4.3.3 ***Wafer Breakage***

A few wafers were broken during handling or processing as they moved through the various process steps. None of the 100 or 200 mm wafers were broken. All of the losses occurred on 150 mm wafers, particularly those that had been back-ground by the manufacturer to reduce their thickness. The preferred approach is to delay back-grinding until the ChipSeal processing is complete.

9.5 *ChipSeal Wafer Processing and Yield Assessment Conclusions*

A broad variety of both commercial and proprietary devices were successfully processed using the ChipSeal technology without unique process refinement specific to device function or geometry. Single, double and triple level metal device structures were processed with gate geometries that ranged from 2 to 0.5 µm, on wafer diameter sizes of 100, 150 and 200 mm. Sarnoff processed most wafers with the dielectric passivation, but the 200 mm wafers were processed through a combination of Dow Corning's ILD customer for FOx, within Dow Corning's Application Center for SiC and by MCNC for patterning and etch. Bumping was performed by a commercial bumping company or, in the case of solder bumping, performed by MCNC. Given the logistics involved for all of these wafers, only a few wafers were damaged during processing, which had a minor impact on wafer yield, and were typically due to the wafer fragility caused by backside thinning.

Digital, analog and test device wafers, with functions that ranged from amplification to logic to memory, were selected to demonstrate compatibility of the ChipSeal technology with devices having intrinsic stress, thermal conditioning and electron charge sensitivities. In addition, radiation hardened devices (SOS) were also processed due to their unique challenge and process complexity. In all cases, material and process compatibility was successfully demonstrated through device yield and failures associated with the ChipSeal processing were negligible or statistically insignificant.

10. Evaluation of ChipSeal Processed Die in Multichip Modules

Upon completion of the device compatibility assessment, the commercial devices were prepared for integration into two MCM designs that were previously discussed. This work was completed under a collaborative IR&D effort between Dow Corning and Rockwell Collins in order to evaluate the ChipSeal processed devices in functional MCM-L applications.

10.1 *Assembly and Test Plan*

Environmental reliability evaluations were conducted on the two MCM designs discussed previously. The demonstration modules were constructed using the six commercial devices listed in the previous process compatibility assessment. The data accumulator module contained 10 analog chips and the GPS module contained 6 digital device chips built on laminate substrates. Each module was to be built in two configurations (with wire bond or flip-chip interconnects) and were to be tested with and without epoxy encapsulation (gob top or underfill). Both control (unprocessed) and ChipSeal processed versions of each module were evaluated. The preparation and test plan is shown in the Figure 49.

10.2 *KGD Screening*

To minimize premature failures and assure high module assembly yields, all of the die to be used in the modules were put through KGD screening. Those intended for wire bond assembly were mounted on temporary carriers using the Chip Supply SofTAB® bonding technique. Those intended for flip-chip assembly were bonded on temporary laminate carriers using the MCNC proprietary BATS® process. Following the KGD screening, the ICs were removed from the carriers using the appropriate dejoining methods for each process.

The actual KGD yields are proprietary since the results reflect on the robustness of each manufacturer's device. Overall, the screening process eliminated about 10 percent of the die designated for module assembly. For individual die types, the fallout ranged from a low of 5 percent to a high of 23 percent. Approximately 6 percent more ChipSeal parts failed the screening than did the standard die. However, since the standard deviation in failure rate between groups was over 8 percent, the difference is probably not statistically significant.

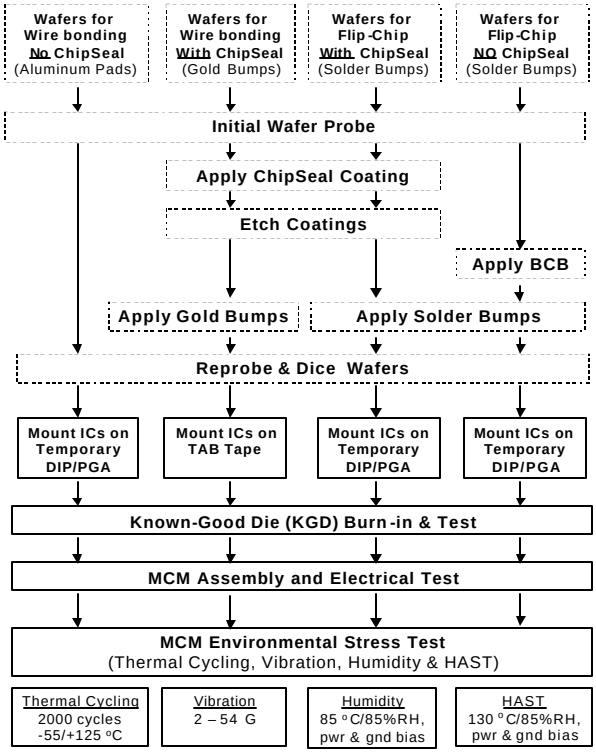


Figure 49. Module Test Plan

10.3 *Module Test Results*

Only the results on the wire bond module configurations are reported. Thermal mismatch and/or fatigue problems encountered during carrier assembly and KGD testing of the solder bumped die precluded completion of assembly and testing of the flip-chip modules. A total of eight test cells were required to evaluate all of the various wire-bond module assembly combinations, as shown in Table 36.

Table 36. Module Packaging Configurations Evaluated; Wire-Bond

Test Cell	MCM Type	Circuit Type	Interconnect	Wafer Process	Module Encapsulant
1	Data Accumulator	Analog	Wire-bond	None	None
2	Data Accumulator	Analog	Wire-bond	None	Epoxy
3	Data Accumulator	Analog	Wire-bond	ChipSeal	None
4	Data Accumulator	Analog	Wire-bond	ChipSeal	Epoxy
5	GPS	Digital	Wire-bond	None	None
6	GPS	Digital	Wire-bond	None	Epoxy
7	GPS	Digital	Wire-bond	ChipSeal	None
8	GPS	Digital	Wire-bond	ChipSeal	Epoxy

10.3.1 Thermal Cycling

The thermal cycle testing consisted of 1 hour cycles between –55 and +125 °C. Two MCM from each of the test cells were evaluated.

For both module types, all four versions (with/without ChipSeal and with/without encapsulant) survived the 2000 cycles essentially without failures. One data accumulator control module (without ChipSeal and without encapsulant) experienced failure at one wire bond, which was traced to an initial bonding defect.

These results establish that both the ChipSeal process materials and the encapsulant materials are robust enough to pass the cycling tests without evidence of cracking, loss of adhesion or other degradation. The large die, that were encapsulated on the GPS modules, all had sufficient integrity to withstand the cycle tests with no degradation of the wire bond interconnects even for die sizes ranging up to 0.4 inch square and I/O counts greater than 200.

10.3.2 Vibration Testing

The vibration tests were designed to aggravate highly stressed areas in the module assemblies resulting from excessive inertial loads or deflections. Stepwise, increasing G-loads ranging from 2 to 54 G_{rms} were applied to each module for 15 minutes, followed by electrical testing. Two modules from each test cell were evaluated.

For the data accumulator modules, only one unencapsulated control module experienced an interconnect failure between the IC and the module substrate at the 6 G_{rms} level. This was attributed to the breakage of an unsupported gold wire. The other ICs on this module and all of the other modules remained functional up to 44 G_{rms}. Spurious failures of the solder joints between the module substrate and the test board were encountered but, after repair, no further failures were encountered.

For the GPS modules, no vibration failures were encountered up to the highest exposure level of 54 G_{rms} .

These results indicate that the ChipSeal metallization is sufficiently robust to withstand the high G-loads and vibrations expected for military and aviation applications.

10.3.3 High Humidity Testing

High humidity testing was conducted at 85 ºC and 85 percent RH with a continuous 5 volt bias on the power and ground leads. The power dissipation was less than 30 milliwatts, so there was no significant die heating.

All of the ChipSeal processed devices assembled onto the data accumulator modules (with or without encapsulation) passed the 1000 hour exposure. One encapsulated control module showed complete failure after 400 hours of exposure. Two other encapsulated control modules and the single bare die control module also survived the 1000 hour exposure. For an

encapsulated sample to have poorer corrosion resistance than a bare sample is not a typically expected outcome. However, the encapsulant epoxies, typically acid anhydride cured, have sufficient contents of ionic impurities to accelerate corrosion within a moisture – bias test over that of the bare die counterpart in high humidity conditions.

For the GPS modules, a higher purity grade of encapsulant was used. Some parameter shifts were detected for the control modules but no massive corrosion failures were observed. The bare control modules showed the highest number of shifts, starting as early as 200 hours of exposure. All of the ChipSeal modules passed the 1000 hour exposure with no failures.

10.3.4 HAST Exposure

The HAST assessments were performed to simulate long term field corrosion and diffusion failure mechanisms. The tests were conducted at 130 ºC and 85 percent RH for up to 1000 hours. The same voltage bias conditions were used as in the 85 ºC / 85 percent RH test (+5 volts between power and ground). HAST exposures were found to be the most discriminating reliability test in terms of the effectiveness of the die protection methods being evaluated.

For the data accumulator modules, the results are shown in Figure 50. All of the encapsulated modules (both the control and ChipSeal modules) failed by the end of the first 200 hour exposure. The bare die modules all passed the 200 hour exposure but were showing progressively increasing failures up to the 750 hour test termination point. The results are similar to those for the high humidity tests in that the corrosion failures are much higher for the encapsulated modules than they are for the bare die modules. This result is not surprising to those experienced in humidity or HAST testing of gob-top encapsulated die because of the higher corrosive content of the acid anhydride cured materials, as compared to molded epoxies. Thus, encapsulated die tend to fail much earlier than die molded in plastic packages.

In the encapsulated control modules, the dominant failure was anodic corrosion of the aluminum pads at the positively biased locations. In severe cases, the corrosion extended under the passivation along the aluminum traces. In the bare die control modules, the dominant failure was corrosion of the aluminum pads at the negatively biased locations. Also, corrosion was occasionally observed in central areas of the die for both types of control modules, indicating that the primary passivation on some die contained pinhole or other defects.

For the ChipSeal protected modules, the failure rate was much higher than expected, particularly for the epoxy encapsulated samples. Examination of the samples showed that there were no pinhole corrosion failures, but that there was a definite corrosion of the UBM at the bondpads. Two types of protective metallization were used in the program (from two different vendors). The thin gold pads over TiW applied by Sarnoff in Phase I worked very well, as seen by the previous data. The electroplated gold bumps over TiW used in Phase II was very mechanically robust and passed the high humidity tests, but lose adhesion between the gold and the UBM during the HAST testing. The electroplated gold bumps separated from the TiW diffusion barrier and lifted from the pads. Once the gold lifted, corrosion proceeded rapidly through the barrier material and into the aluminum metallization on the ICs. Since all of the ChipSeal ICs were fabricated with the gold bumps, all experienced the same failure.

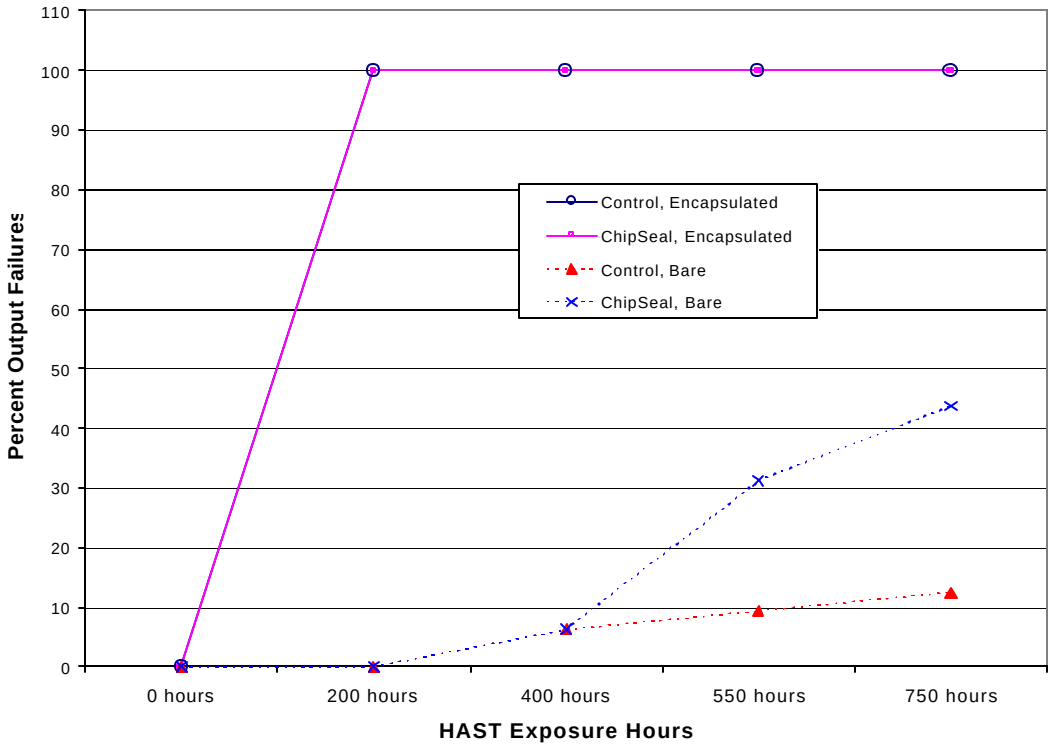


Figure 50. HAST Failures in Data Accumulator MCMs

For the GPS modules, a similar behavior was observed (Figure 51). The encapsulated components failed at about the twice the rate of the unencapsulated components. The same corrosion mechanisms were observed for these modules as the data accumulator modules. Pinhole corrosion was observed for the control modules (original passivation) but none was observed for the ChipSeal processed modules, thus indicating that the ChipSeal coatings were indeed providing hermetic-like protection of the internal areas of the die. At the bondpads, the failures were again the corrosion of the TiW UBM accompanied by the lifting of the gold bumps. At the most severe corrosion sites, no residue of the TiW was observed on either the gold bump or the pad surface. These results suggest that a more reliable metallization, particularly the UBM, is needed to provide hermetic-equivalent performance for encapsulated COB type of assemblies. However, it must be remembered that two factors were different for the module testing: 1) a different source was used for the metallization, and 2) the HAST exposure was done in the presence of contaminants from both the substrates and encapsulants that were not present in Phase I tests.

In an attempt to resolve the metallization source or type issue, SRAM test modules were assembled and exposed to HAST conditions using both die gold bumped from the commercial bumping service and die metallized at Sarnoff. After 200 hours of testing under the same conditions, both metallization types exhibited separation and lifting of the gold at the UBM interface. These results suggest that neither the company providing the metallization services nor the SofTAB bond-debond process contributed directly to the reduction in HAST reliability.

Ion beam milling and SEM analyses were conducted at WPAFB on both HAST exposed and unexposed gold bumped die. For the unexposed sample, intimate attachment of the gold bump

to the UBM was observed. A small (1 µm) undercut of the TiW existed at the perimeter of the bump. For the HAST exposed sample, a pad location was used where the bump had not lifted. A definite void or separation was observed at the interface between the gold and the TiW UBM. The cause of the void or separation is not known.

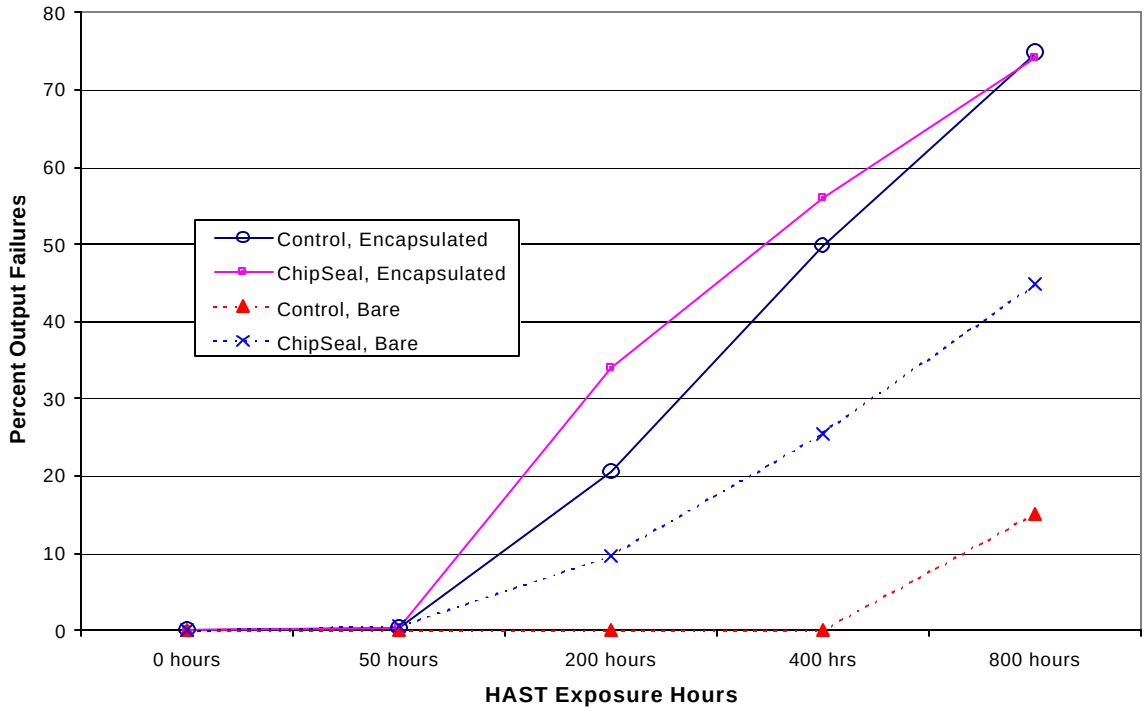


Figure 51. HAST Failures for the GPS MCMs

10.3.4.1 ***Observations on the Bondpad Failures***

1. The separation occurred on all IC types used in the modules and appeared to occur randomly, independent of bias polarity.
2. The separation occurred at the interface between the bottom of the gold bump and the top of the TiW UBM. With longer exposure after separation, the UBM is eventually corroded away.
3. Mechanical tests indicate an initial strong bond between the gold and UBM that is not affected by temperature cycling or vibration exposures.
4. Only HAST exposures resulted in bump failures.

10.4 *MCM Evaluation Conclusions*

A comparative assembly and reliability test matrix was completed using two different MCM designs, a data accumulator and GPS, which were assembled using laminate substrates with either bare (uncoated) or ChipSeal coated die. All die were subjected to KGD testing prior to MCM assembly and a proportionate number of MCMs had the die encapsulated in epoxy. No significant differences in KGD or MCM yields were observed. ChipSeal coatings were found to be compatible with standard KGD testing and MCM assembly processes.

The MCM-L designs were demonstrated to be mechanically robust in severe environments, as evidenced by the temperature cycling and vibration tests. However, ChipSeal coated die provided a significant improvement in high humidity protection. All ChipSeal modules survived 1000 hours of 85 ºC/85 percent RH/5 V bias, whereas 10 to 30 percent failures were observed for MCMs with bare (uncoated) die. HAST exposure provided the greatest degree of differentiation between the various test configurations. The ChipSeal passivation coatings were found to eliminate pinhole corrosion failures on the central die region of the devices. However, the metallization system did not provide the level of protection needed to protect the aluminum bondpads from corrosion. The ChipSeal MCMs showed single or multiple open circuit electrical failures and were attributed to corrosion of the underlying aluminum bondpad resulting in the separation of the gold bump from the TiW barrier layer. The control MCMs showed failures that were attributed to severe corrosion of the aluminum bondpads and circuit traces under the original passivation. Further failure analysis is required to fully understand the failure mechanism on the ChipSeal coated devices.

11. Evaluation of ChipSeal for Commercial PEMs

One of the devices from Phase II was selected for assembly, plastic encapsulation, and reliability testing in a cooperative effort with the device manufacturer. The device chosen was the microprocessor procured from Rockwell Semiconductor. This is a 0.6 µm CMOS device having 100 I/Os and a 0.180 by 0.185 inch die size. The objective of this effort was to demonstrate the compatibility and relative reliability between the ChipSeal and standard devices in commercial, molded plastic packages.

11.1 *Assembly and Test Plan*

Out of the original group of 10 wafers, one control wafer and one ChipSeal wafer were designated for encapsulation and test. The process flow and test plan is shown schematically in Figure 52. After the post-ChipSeal wafer yield probe at Chip Supply, both wafers were shipped to Rockwell for assembly. Approximately 1000 die from each wafer were packaged in the Rockwell plant using production equipment and materials for dicing, die attach, wire bonding, and molding. The package configuration was a 100 lead PQFP (Plastic Quad Flat Pack) measuring 14 by 20 by 2.8 mm. Approximately 500 parts from each wafer were electrically tested. The packaging yield for each group differed by less than 1 percent. The data suggests that the ChipSeal Hermetic Coatings were compatible with high volume plastic packaging equipment and processes.

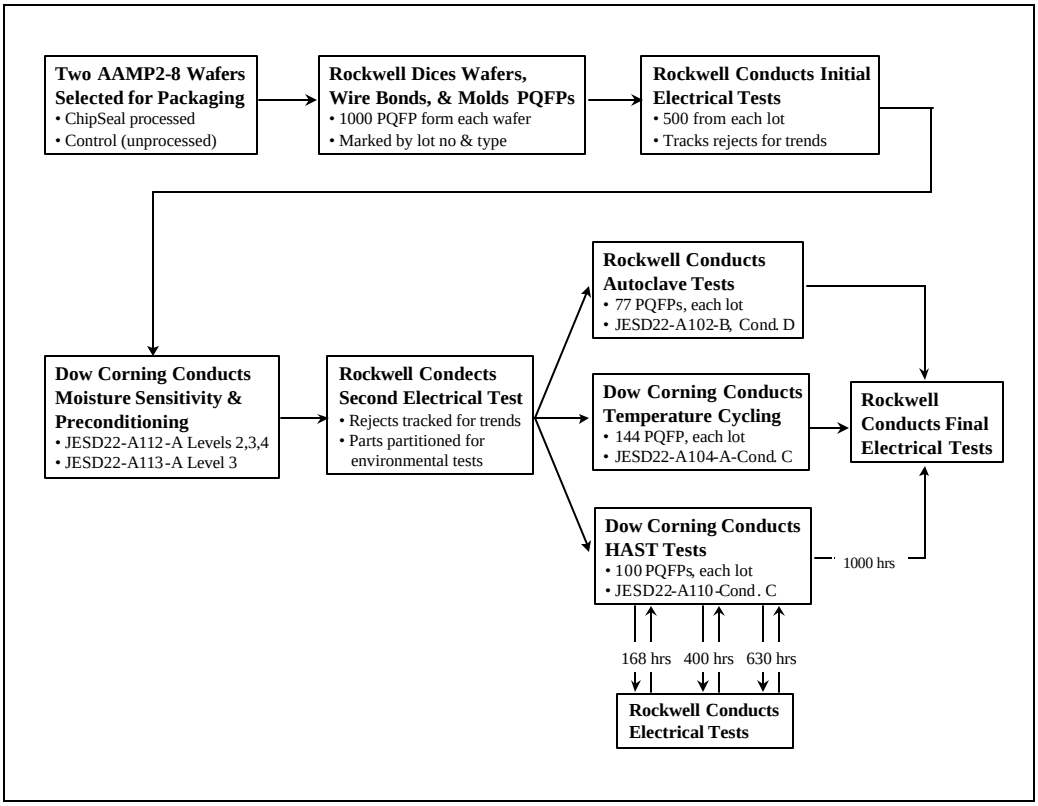


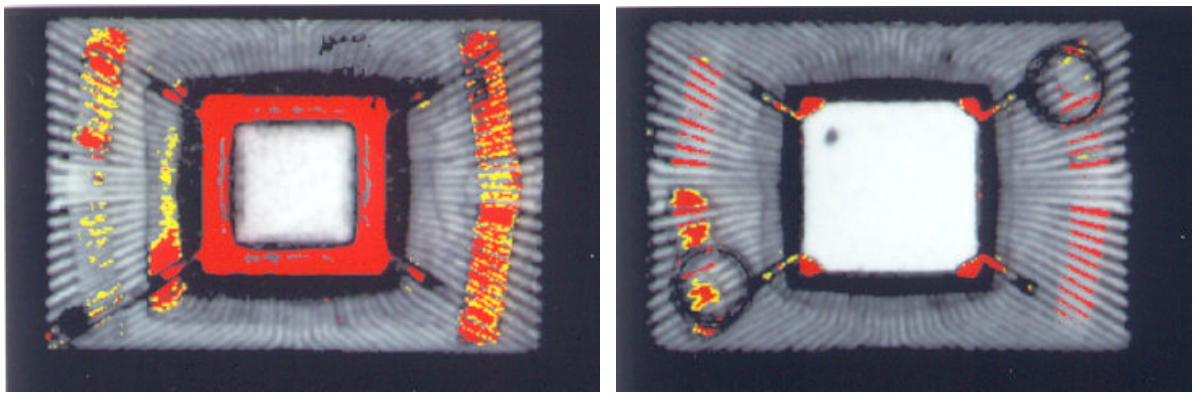
Figure 52. PQFP Process Flow and Test Plan

11.1.1 Moisture Sensitivity Evaluation

Thirty-five devices of each type were submitted for moisture sensitivity evaluations at Levels 2, 3, and 4 using the JEDEC method A112:

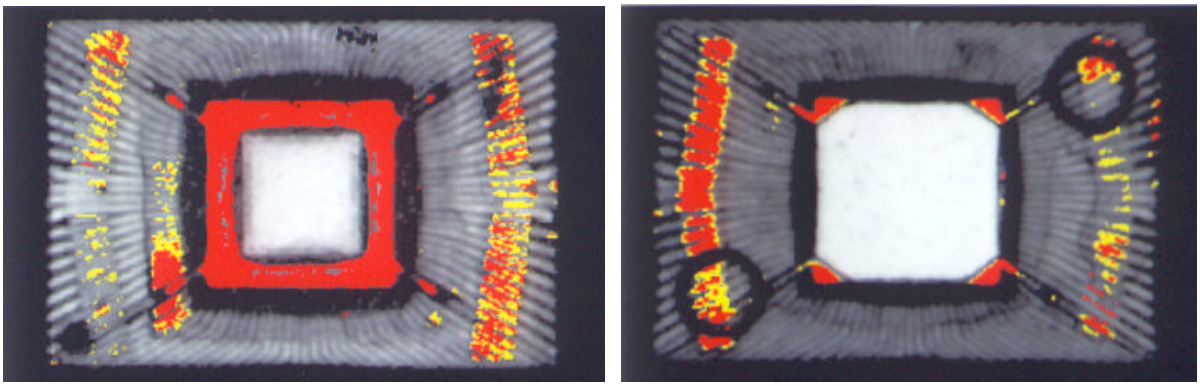
Level 2:	168 hrs (85 ºC/60 percent RH)
Level 3:	220 hrs (30 ºC/60 percent RH)
Level 4:	96 hrs (30 ºC/60 percent RH)

The pre and post package integrity was assessed using C-mode scanning acoustic microscopy (CSAM) to identify any delaminations in the structure. Figures 53 and 54 show the typical CSAM images for the Level 3 exposures. No significant differences were revealed; both die types qualified at Level 3. The results indicate that the ChipSeal coating did not degrade the bond between the encapsulating compound and the die interface. The delaminations that did occur were generally isolated to the backside of the die paddle or lead frame areas, as evidenced by the red coloration shown in the images.



Top Bottom

Figure 53. Typical CSAM Image for ChipSeal Processed PQFP After Level 3 Moisture Sensitivity Evaluations



Top Bottom

Figure 54: Typical CSAM Image for Control PQFP After Level 3 Moisture Sensitivity Evaluations

11.1.2 Preconditioning

Based on these results, approximately 400 parts from each group were submitted for preconditioning at JEDEC Level 3 (see Figure 55 for preconditioning conditions). The preconditioning simulates conditions for surface mount assembly processes. After exposure, each part is visually inspected and electrically tested. There were no visual rejects and only one electrical (functional) failure of a ChipSeal part after preconditioning. The parts were then subdivided into groups for the subsequent autoclave, temperature cycling, and HAST testing, as shown in the test flow diagram (Figure 52).

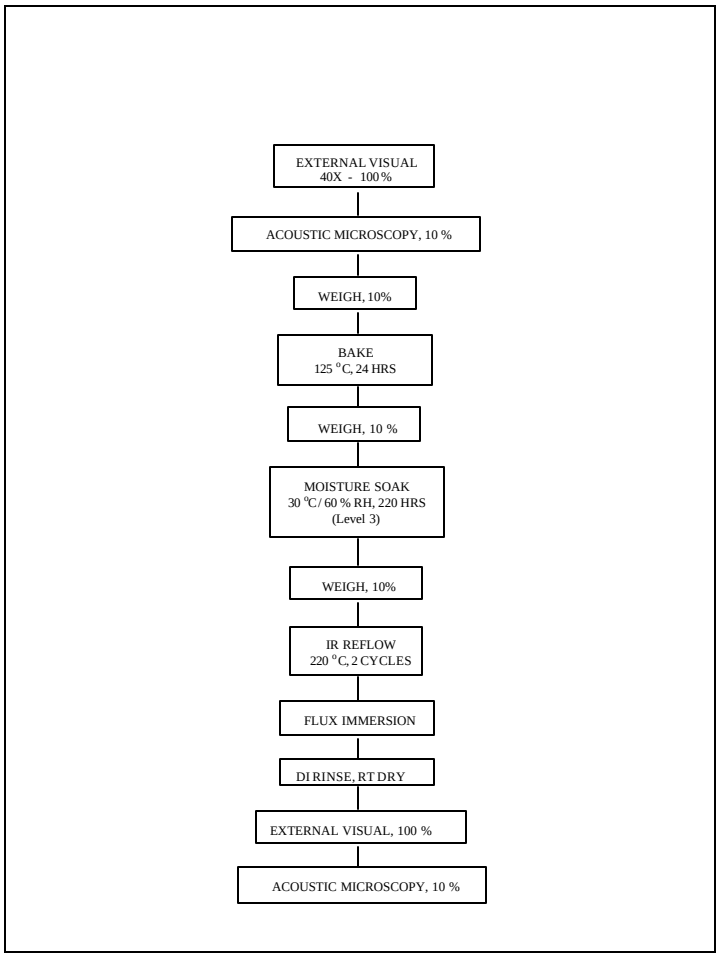


Figure 55. AAMP 2.8 PQFP Preconditioning Parameters
JESD22-A113-A (Modified)

11.2 *Environmental Reliability Test Procedures*

Seventy-seven parts of each type were subjected to an unbiased autoclave exposure at 121 °C, 15 psig, for 168 hours (JESD22-A102- Cond D), and 144 parts each were subjected to 2000

temperature cycles at -65 to + 150 °C. There were no electrical failures for either group after exposure.

One hundred parts of each type were subjected to HAST testing at 130 °C, 85 percent RH for 1000 hours (JESD22-A110-Cond. C). The parts were subdivided into two groups using two different bias schemes as indicated in the HAST test plan (Figure 56). The parts were electrically tested after intervals of 168, 400, 630, 1000 hours.

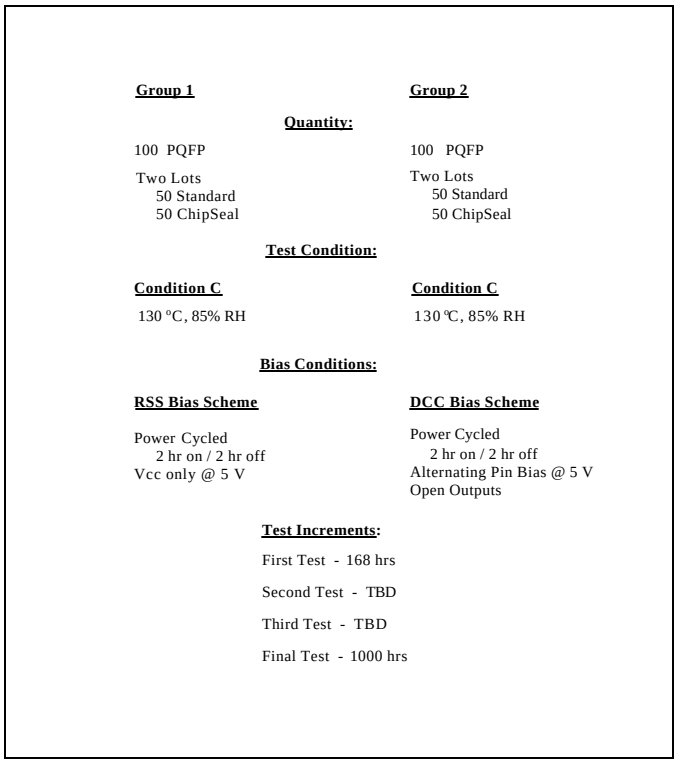


Figure 56. AAMP 2.8 PQFP HAST Test Parameters
JESD22-A110-Cond. C

11.3 *Test Results*

Only two ChipSeal and one control samples failed after the 1000 hour increment. The control part failed for intermittent continuity and some function tests. The ChipSeal parts failed various leakage currents and functional tests.

Since the above results were inconclusive at 1000 hours, the parts were subjected to an additional 500 hours of HAST exposure at the same conditions. The additional exposure so severely corroded the pins that they would not make contact in the test sockets. After vapor cleaning and replating the parts were retested. Two parts had broken leads and could not be tested. Thirty-two parts failed various electrical tests, mostly continuity. However, the cleaning removed the serial numbers, thus making it impossible to identify the parts directly. The electrical failures were subsequently decapped to distinguish the part types. The results are summarized in Table 37. The number of failures, after 1500 hours of exposure, were nearly identical (17 ChipSeal and 15 standard devices respectively).

Table 37. HAST Test Summary for PQFP Packaged AAMP 2.8 Microprocessor

		Configuration						
		ChipSeal			Standard			Grand Total
		Bias Scheme			Bias Scheme			
Test Increment		DCC	RSS	Total Pkgs	DCC	RSS	Total Pkgs	
1000 Hr	Start	50	50	100	50	50	100	200
	Elec.Fails		2	2		1	1	3
	Good	50	48	98	50	49	99	197
1500 Hr	Start	50	48	98	50	49	99	197
	Broken	-	-	1 *	-	-	1 *	2
	Elec Fails	-	-	17	-	-	15	32
Total	Elec. Fails			19			16	35
	Total Good			80			83	163

* Identity of broken pieces unknown -- assumed one of each type.

11.4 *PEM Conclusions*

A high volume commercial device, the AAMP2-8 microprocessor, was used in a comparative test matrix to assess the compatibility and relative reliability between ChipSeal coated and standard devices in commercial, molded plastic packages. Assembly and plastic encapsulation was completed on a statistically significant quantity of devices with no differences in handling or processing through the automated packaging process. Results from the initial electrical tests illustrated that the ChipSeal processing was compatible with and did not degrade the electrical performance of the microprocessor, when packaged in Rockwell's standard production PQFP package.

Subsequent moisture sensitivity, preconditioning and reliability testing was unable to differentiate reliability improvements of the ChipSeal coated devices over Rockwell's standard device. The high integrity, robust design and moisture resistance of the AAMP2-8 molded package precluded distinguishing the devices from each other and therefore, any minor differences in the number of failures were statistically insignificant.

12. Program Conclusions and Recommendations

An advanced inorganic passivation system, known as ChipSeal Hermetic Coatings, was developed and deposited at the wafer level from "molecular designed" silicon materials using standard semiconductor processing technology. This passivation was combined with a high reliability noble bondpad metallization system to produce a more robust IC for advanced packaging applications.

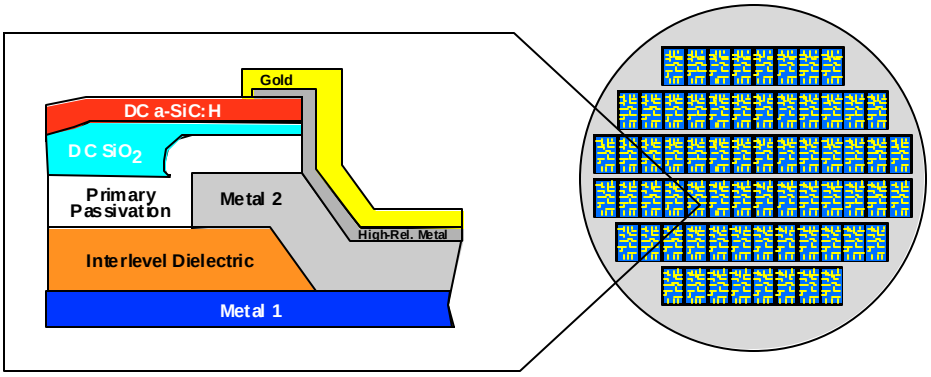


Figure 57. Manufacturing Semiconductor Devices with Built-in Hermetic Equivalent Reliability

Phase I successfully demonstrated "proof-of-concept" of the hermetic equivalence afforded by the ChipSeal coatings when applied to 1.5 µm BiCMOS gate arrays. A comparative reliability assessment was completed on plastic SMT (300 mil wide, 95 mil thick) and bare chip devices using both MIL-STD-883 screening and qualification tests and severe JEDEC preconditioning and test methods. The most discriminating test was found to be 1000 hours of HAST exposure at 140 ºC (temperature/humidity/pressure and bias testing). The data clearly demonstrates the hermetic-equivalent performance of both PEMs and bare IC die when devices are processed with ChipSeal. In addition, initial data was generated that indicates that the ChipSeal technology is compatible with flip-chip solder bumping.

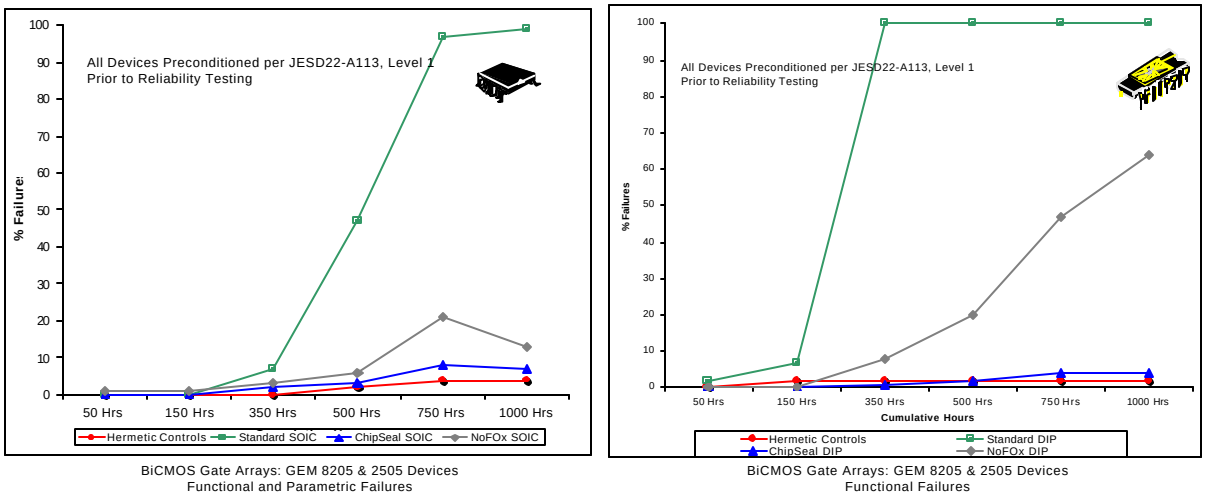


Figure 58. Performance of Plastic SOICs and Bare Die in 140 °C HAST

Phase II successfully demonstrated the compatibility of the ChipSeal technology to a variety of device types; approximately 100 wafers of 6 different commercial and 4 proprietary devices were processed and tested. The devices were obtained from a variety of merchant IC suppliers, chosen on the basis of function, gate geometry, and application which ranged from simple linear amplifiers to high speed digital microprocessors. In addition, a variety of metallization systems were used with the ChipSeal technology, some from third party merchant suppliers, illustrating compatibility with both gold and solder bump processing. All of the processed wafers showed some overall decline in yield that varied widely by device type and metallization. In general, the net change in yield relative to the control wafers was small (< 5 percent) and considered within the variability of the probe process itself. The result indicates that the ChipSeal processing is compatible with a multiplicity of device types and any effect on device yield is within the variability of the test method.

A 0.6 µm CMOS microprocessor in a 100 lead PQFP format was chosen for comparative packaging and reliability assessments in cooperation with the device manufacturer, Rockwell Semiconductor. The plastic packaging yield differed by less than 1 percent and moisture sensitivity evaluations per JEDEC Method A112, Level 3, indicated that there was no difference in the effect of the ChipSeal coating on the adhesion between the encapsulation compound and the die surface. Parts were preconditioned (Level 3) and subdivided into three statistical groups for unbiased autoclave (121 ºC/168 hours), temperature cycling (-65 to +150 ºC, 2000 cycles), and HAST testing (130 ºC, 85 percent RH, 1500 hours). There were no electrical failures as a result of the autoclave and temperature cycling exposures. The HAST exposure did produce failures, a total of 16/100 versus 19/100, with almost identical failure rates for both the control and the ChipSeal groups respectively. In summary, the low number of total failures and the small difference between groups render the results inconclusive. ChipSeal processing did not degrade the intrinsic performance, nor did it enhance the reliability for this particular "highly reliable" device. The overriding factor may be the very high integrity and moisture resistance of this particular manufacturer's package design and process controls.

A comparative MCM evaluation, conducted as an adjunct activity by Rockwell Collins and Dow Corning, successfully demonstrated KGD integration, module assembly and reliability effectiveness of the ChipSeal technology. All MCMs used a combination of SMT devices and bare die, with and without epoxy encapsulants and were subjected to various reliability tests including vibration (incremental exposures up to 53 G_{rms}), temperature cycling (1000 cycles, –55 to +125 °C), and high humidity (up to1000 hours, 85 °C/85 percent RH/5 V) tests. There were no failures attributable to the ChipSeal processing. For the high humidity test, ChipSeal protected ICs survived 1000 hours of exposure without failure, while the control modules experienced 10 to 30 percent failures during the same exposure. In addition, HAST exposures (up to 750 hours, 130 °C/85 percent RH/5 V bias) were conducted and revealed more discriminating results. Epoxy encapsulated die on the data accumulator modules, for both the ChipSeal and control modules, all failed within the first 200 hours of exposure; unencapsulated die modules revealed significant failures not occurring until 400 hours of exposure. The ChipSeal modules showed single or multiple open circuit electrical failures and were attributed to corrosion of the underlying aluminum bondpad and separation (lifting) of the gold bump from the barrier metallization (TiW). For the control modules, the failures were attributed to severe corrosion of the aluminum bondpads that, in some cases, extended under the passivation and along the die traces. Corrosion was also observed in central regions of the die, attributed to

flaws in the primary passivation, that were not observed for the ChipSeal coated die. A similar situation was observed for the GPS modules.

The module data suggests that a contributing factor to the HAST failures appears to be the use of epoxy encapsulants (acid anhydride curatives) or plastic laminate substrates. This has not been well documented in the literature, since HAST is a relatively new reliability test method, especially for MCMs, but is clearly an area requiring follow-up. An underlying concern is that the high reliability metallization did not provide the level of protection expected when used in a direct chip attach architecture. Multiple hypotheses could account for the failures that were caused by the ingress of moisture and corrosive ions, as follows:

- Residual contaminants from wafer processing/etching.
- Contamination of the aluminum pad prior to deposition of the metallization system due to handling, packaging and shipping between processing facilities.
- Degradation of the interface between the plasma-SiC and the metallization system caused from the undercutting of the TiW during wet etch processing resulting in a buildup of localized high stresses along the interface.
- Prior experimental data showed the importance of process control with respect to the amount of nitrogen moiety within the TiW barrier layer. Nitrogen can backfill into the sputtering chamber and become incorporated into the TiW film (i.e. TiWN) leading to a reduction in adhesion properties to both the gold layer as well as the substrate.
- Film stress of the deposited TiW metallization differed significantly between runs from the same sputtering tool as well as from different tools. High film stress leads to delamination (adhesion loss) of the films at the interface.
- Probe marks observed on all wafers prior to processing, which reduces the coverage and effectiveness of the TiW barrier layer. Gold in direct contact with aluminum produces intermetallic formation (Kerkendall voiding) and is more susceptible to corrosive attack under adverse conditions.
- Degradation of the metallization stack caused from KGD soft TAB bond / de-bond processing.

In the hypotheses cited, moisture and ionic ingress at the metal-dielectric interface or within the metallization stack can contribute to the degradation of the electrical contact. There is insufficient data to substantiate the MCM failures at this time; additional effort is required. Lack of corrosion failures within the central areas of the ChipSeal processed die indicates that the ChipSeal technology can provide the protection desired.

In conclusion, the ChipSeal inorganic sealing technology has been shown to provide hermetic-like performance in device reliability and is invariant to PEM and MCM packaging formats. The ChipSeal dielectric coatings were integrated into the device passivation process using existing IC fabrication equipment and was proven to be a better IC passivation than the existing plasma-SiOx/SiN stack. ChipSeal was shown to be compatible with a variety of chip interconnection schemes including wire bonding, flip-chip and TAB configurations for MCM and COB applications. The inherent versatility of this proven technology enables the component or system engineer the ability to integrate new device/packaging technology without sacrificing reliability.

The advantages of the ChipSeal technology are as follows:

Technology

Advanced Inorganic Dielectric Passivation
- Spin-on, low dielectric constant, planarizing SiOx dielectric layer.
- PECVD barrier, low dielectric constant a-SiC:H dielectric layer.

High Reliability Metallization
- KGD Compatible
- Gold Bumps
- Flip Chip Solder Bumps
- Thin Film Gold Bondpads

Wafer Level Processing
- Leverages existing IC fabrication equipment
- Leverages existing IC infrastructure.

Application

Applicable to a range of semiconductor and device types including Si, GaAs and SOS.
Hermetic sealing is performed at the wafer level in a cleanroom environment using standard semiconductor processes and equipment.
Robust IC protection for ruggedized applications.
Dual Use.
Lower cost compared to external packaging solutions.
Invariant to package design.

12.1 *Recommendations for Future Work*

The following areas have been identified and recommended for further development:

1. Determine the exact mechanism of the corrosion failures observed in the MCM evaluations.
2. Investigate barrier layer integration:
   a) Run-to-run variability
   b) Tool-to-tool variability
   c) Key contaminants
   d) Interfacial and microstructural properties
   e) Vertical sidewall etch processing to prevent undercutting.
3. Identify and evaluate alternate metallization systems for use with potentially corrosive encapsulation systems.
4. Investigate integration with flip-chip solder bump:
   a) Nature of many failures was different but the number of failures were similar.
   b) Complete evaluations of flip-chip metallization structures in HAST with and without encapsulants.
5. Reduce process temperatures and integrate ChipSeal into GaAs device manufacturing.

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List of Abbreviations

a-SiC	Amorphous Silicon Carbide
AES	Auger Electron Spectroscopy
ASIC	Application Specific Integrated Circuit
Au	Gold
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
COB	Chip-On-Board
COTS	Commercial-Off-the-Shelf
CSAM	C-Mode Scanning Acoustic Microscopy
CTE	Coefficient of Thermal Expansion
CVBT	Capacitance-Voltage Breakdown Test
Cr	Chrome
Cu	Copper
CVD	Chemical Vapor Deposition
DARPA	Defense Advanced Research Program Agency
DLM	Double Level Metal
DOE	Design of Experiment
D-packages	Ceramic side-brazed cavity package
DC	Direct Current
DCC	Dow Corning Corporation
DIP	Dual Inline Package
DSP	Digital Signal Processor
EDTA	Ethylene Diamine Tetraactic Acid
EMC	Epoxy Molding Compound
FOx®	Flowable Oxide
FC	Flip-Chip
GEM	General Emulation Microcircuit
GPS	Global Positioning System
HAST	Highly Accelerated Stress Test
HF	Hydrogen Fluoride
$HSiO_x$	Hydrogenated Silicon Oxide
I/O	Input/Output
ICDD	International Center for Diffraction Data
ILD	Interlayer Dielectric
IC	Integrated Circuit
IR&D	Internal Research & Development
JEDEC	Joint Electronic Device Engineering Council
KGD	Known Good Die
LOCOS	Local Oxidation of Silicon
MCNC	Microelectronics Center of North Carolina
MCM	Multichip Module
MPSGD	Minimally Packaged Stay-Good Die
NMOS	N-channel Metal Oxide Semiconductor
OpAmp	Operational Amplifier
PEM	Plastic Encapsulated Microcircuit

PDIP	Plastic Dual In-line Package
PECVD	Plasma Enhanced Chemical Vapor Deposition
PQFP	Plastic Quad Flat Pack
PSG	Phosphosilicate Glass
RAM	Random Access Memory
RF	Radio Frequency
RGA	Residual Gas Analysis
RIE	Reactive Ion Etch
RH	Relative Humidity
RWOH or Rw/oH	Reliability Without Hermeticity
SCCM	Standard Cubic Centimeter per Minute
SEM	Scanning Electron Microscopy
SiC	Silicon Carbide
SiN	Silicon Nitride
SiO_2	Silicon Dioxide
SMR	Single Mask Redistribution
SMT	Surface Mount Technology
SOIC	Small Outline Integrated Circuit
SOS	Silicon on Sapphire
SPEC	Surface Protected Electronic Circuits
TAB	Tab Automated Bonding
Ti	Titanium
TiN	Titanium Nitride
TiW	Titanium Tungsten
TiWN	Titanium Tungsten Nitride
UBM	Under Bump Metallization
WAT	Wafer Acceptance Test
WPAFB	Wright-Patterson Air Force Base
XRD	X-Ray Diffraction